

Electronic components & applications

Vol. 3, No 1
November 1980



Electronic components & applications

Volume 3, No. 1

November 1980

Editors

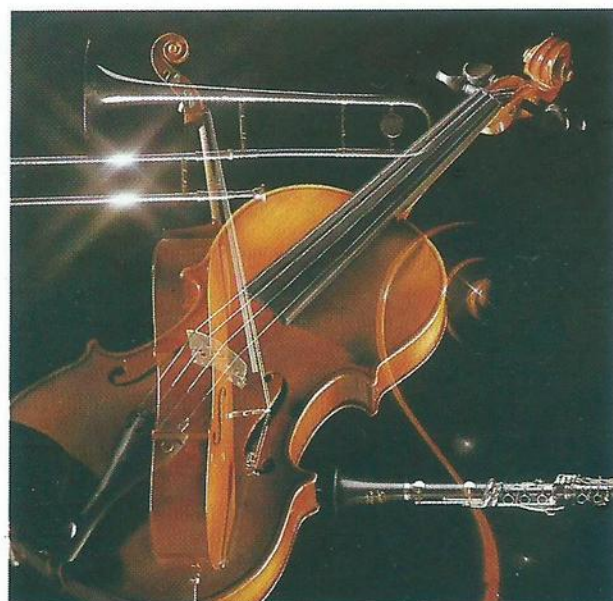
Edmund G. Evans (Mitcham)
William E. Martin (Eindhoven)
Michael J. Prescott (Mitcham)

Design and Production

Cees J. M. Gladdines
Bernard W. van Reenen
Jacob Romeijn
Michael J. Rose

Design consultant

Theo Kentie



A remarkable characteristic of music is its ability to evoke nostalgia. Nostalgia for the time of its composition, for the composer, or performer, or for the occasion we first heard it played. But in his professional capacity, at least, no nostalgia assails the designer of audio reproduction equipment. His thoughts are directed toward the future. Toward the perhaps mythical lure of ideal audio reproduction. In this issue we have an article that will bring the myth somewhat closer to reality. The article concerns a new semiconductor laser for use with the video long player and its audio counterpart the compact audio disc. For audio, the introduction of the compact disc will remove all the noise and distortion currently associated with discs and styli. Myth and reality are steadily merging, but where are we heading? Nostalgia is a compelling force. Will it drive the audio buff of the future to demand circuits that restore the very imperfections we have striven so long to eradicate?

Contents

CQL10 semiconductor laser for information readout	2
Analogue control system for a.c. motor with PWM variable speed drive	6
<i>W. B. Rosink</i>	
Highlight handling with diode-gun Plumbicon [®] tubes	17
<i>A. Franken and W. Lohuis</i>	
Ceramic permanent magnets for d.c. motors	22
<i>H. J. H. van Heffen</i>	
New hybrid stepping motor design	31
<i>B. H. A. Goddijn</i>	
Serial I/O with the MAB8400 series microcomputers	38
<i>A. P. M. Moelands</i>	
Frequency synthesiser using LSI devices	47
<i>P. R. Brennand and B. Murray</i>	
Abstracts	62
Authors	64

Serial I/O with the MAB8400 series microcomputers

Archief
Ir. A.P.M. Moelands

A. P. M. MOELANDS

A microcomputer with a mask-programmed memory is a general purpose device with a dedicated function that is specified by the contents of its ROM. The increasing use of microcomputers in domestic and industrial apparatus, where much of the task is control rather than computation, has led to the requirement for modification of some of the hardware functions of these devices.

The 8400 series* has been developed from the well-known 8048/8021 devices, to provide microcomputers with additional dedicated functions suited to control applications. Architecture and pin layout of the 8400 series are similar to the 8021 microcomputer, while the instruction set is based upon that of the 8048 microcomputer. The 8400 series comprises a range of functionally identical devices offering a variety of ROM and RAM capacities to suit the application.

Serial input/output

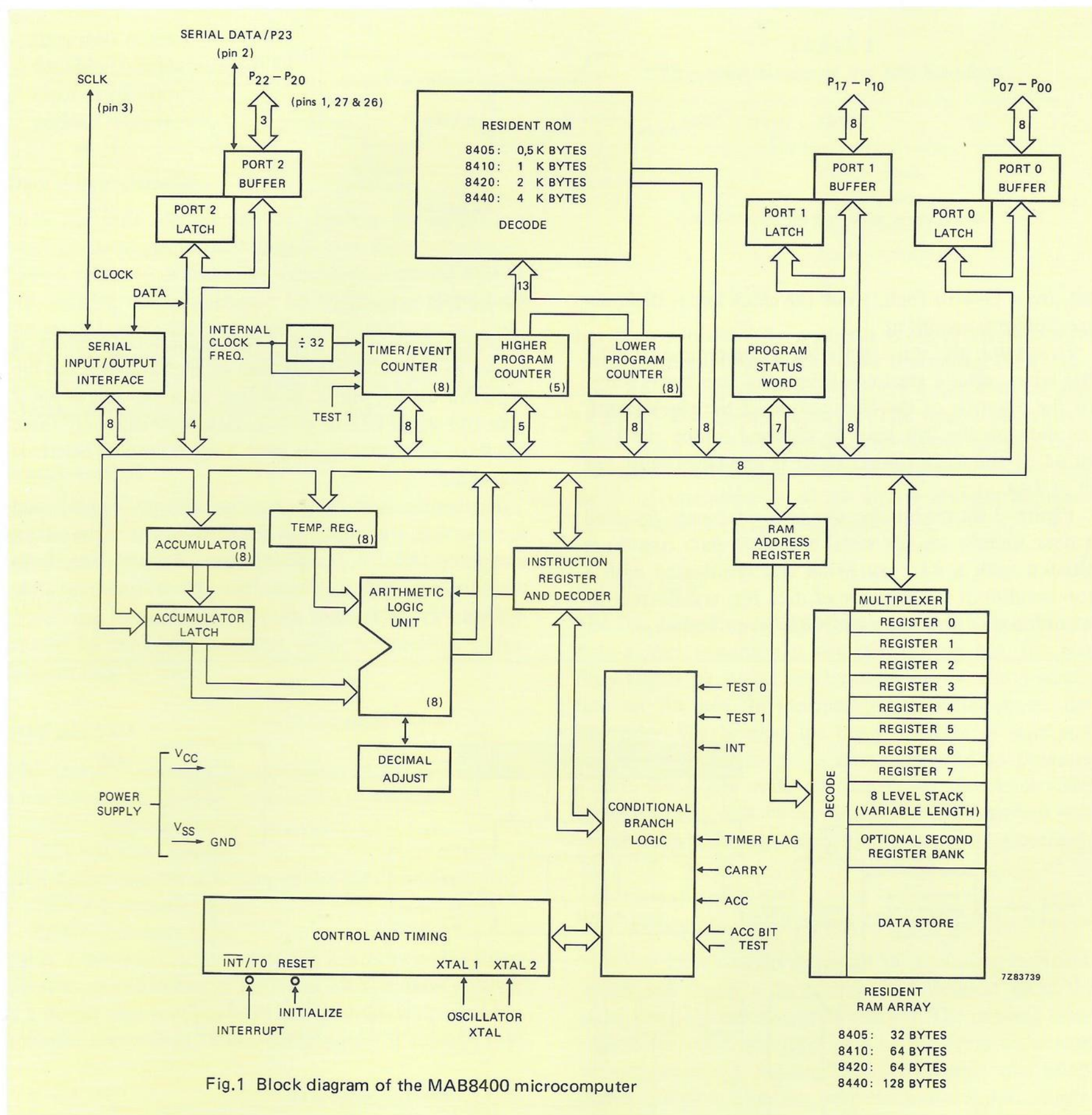
Use of serial data communication between devices greatly reduces the number of connections required, leading to simpler circuit layout and economies in connector size and printed circuit board area. One of the special functions of the 8400 series, the Serial Input/Output (SIO) interface has been designed to eliminate the heavy processing load imposed upon a normal microcomputer performing serial data transfer. The SIO interface can be seen in the block diagram of the 8400 in Fig. 1.

* Detailed information on the MAB8400 series can be found in a separate Technical Publication.

Whereas a normal microcomputer must regularly monitor the serial data bus for the presence of data, the 8400's SIO interface detects, receives and converts the serial data stream to parallel format without interrupting the execution of the current program. Only when the complete byte has been received is an interrupt sent to the microcomputer, which can then read the data byte in a single instruction. Likewise, for transmission, the SIO interface performs the parallel to serial conversion and subsequent serial output of the data while the microcomputer continues with execution of its programmed tasks.

The design of the 8400's SIO system allows any number of 8400 devices to be interconnected by the two-line serial bus. Furthermore, the ability of any two devices to communicate, without the slightest interruption of the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to messages prefixed with its own address or the 'general call' address. The address recognition procedure is performed by the interface hardware so that operation of the microcomputer need only be interrupted when a valid address has been received. This results in a significant saving of processing time and memory space compared with a conventional microcomputer employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcomputers, direct data transfer without addressing can be performed.

The 8400 serial input/output system also provides simple mechanisms for implementation of master/slave operation of devices, acknowledgement of data



reception and an asymmetrical clock signal for use with conventional microcomputer systems. When multimaster systems are used, an arbitration procedure is automatically invoked, thus preventing two or more devices from continuing simultaneous transmission.

Serial data bus

The 8400 serial interface has been designed to work with a serial bus consisting of two bi-directional lines: one for data signals and one for clock signals. A protocol has been defined to allow reliable and efficient operation of this bus:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is High. Changes in the data line while the clock line is High will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: both data and clock lines remain High.

Start data transfer: a change in the state of the data line, from High to Low, while the clock line is High defines the *start* condition.

Stop data transfer: a change in the state of the data

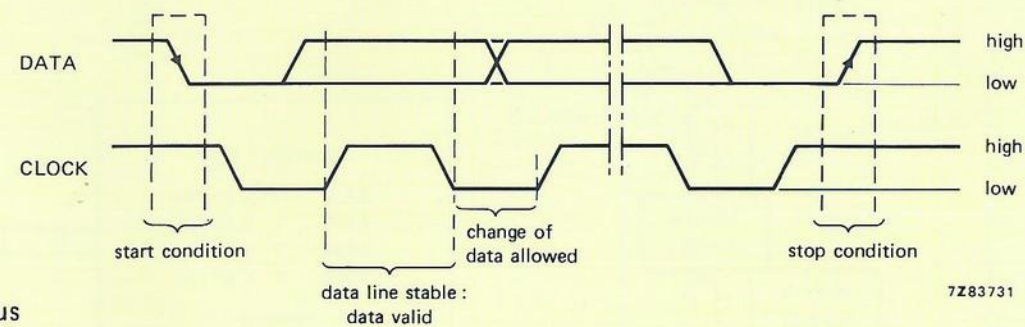


Fig.2 Data transfer sequence on the serial bus

line, from Low to High, while the clock line is High, defines the *stop* condition.

Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Figure 2 illustrates the sequence of events involved in data transfer on the serial bus. Each data transfer is initiated with a start condition and terminated with a stop condition; the number of data bits transferred between the start and stop conditions is not limited.

Serial I/O interface

A block diagram of the 8400 serial I/O interface is shown in Fig. 3. The clock line of the serial bus has the exclusive use of pin 3, while the data line shares pin 2 with I/O signal P23 of port 2. Consequently, only three I/O lines are available for port 2 when the SIO interface is enabled.

Communication between the microcomputer and the interface takes place via the internal bus of the microcomputer and the Serial Interrupt Request line. Four registers are used to store data and information controlling the operation of the interface:

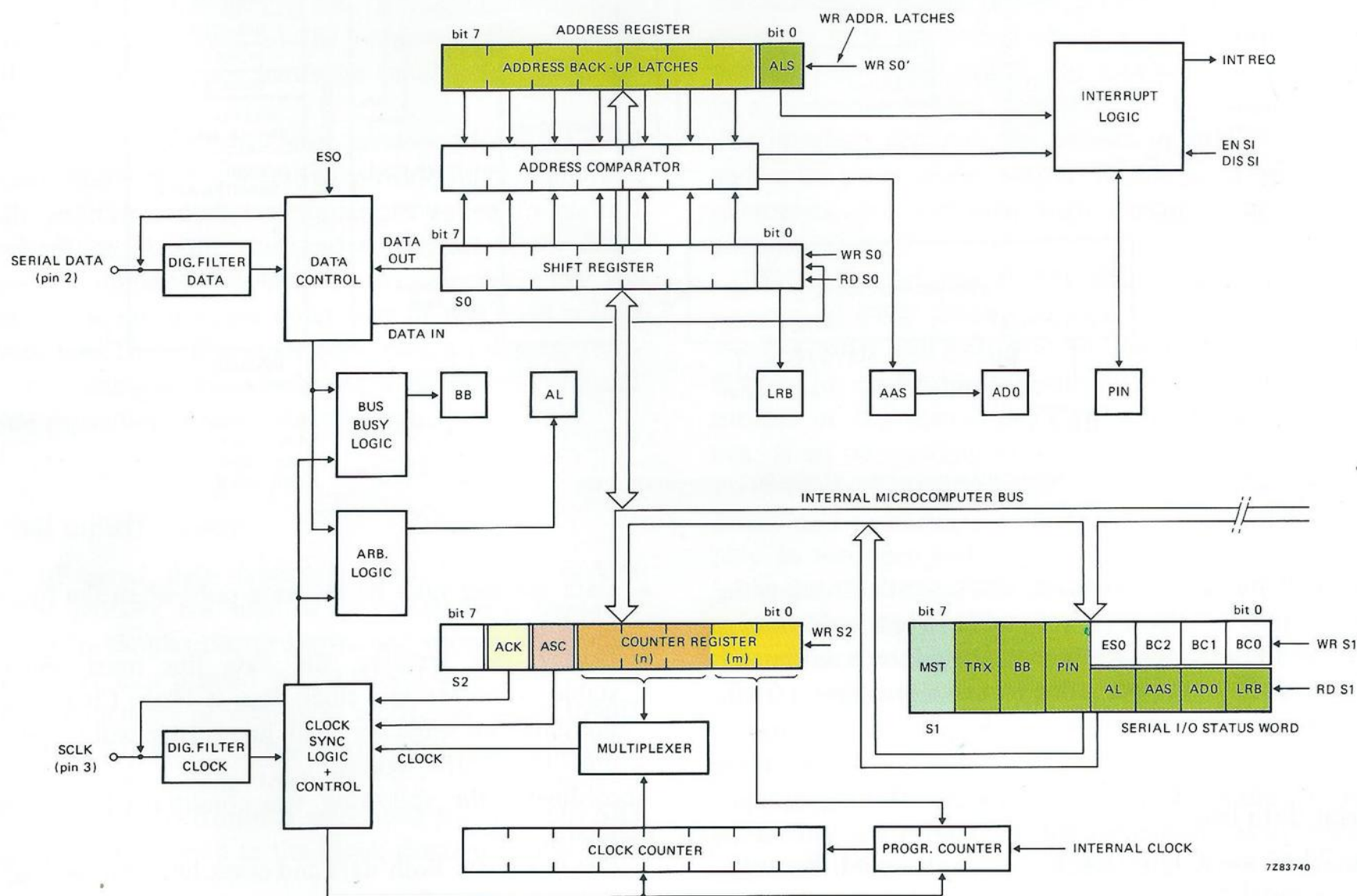


Fig.3 Block diagram of the MAB8400 SIO interface

- data shift register S0
- SIO interface status word S1
- clock control word S2
- address register.

Data shift register S0

S0 is the shift register used to perform the conversion between serial and parallel data format. Data to be transmitted is loaded in S0 by the microcomputer and shifted out serially, most significant bit first. Data received on the serial bus is shifted into S0, most significant bit first. After transmission of a complete byte or reception of a complete data byte, the specific address, or the general address, a pending interrupt is generated.

Status word S1

S1 provides information for the microcomputer about the state of the interface and stores interface control information from the microcomputer. The bit allocation of S1 is shown in Fig. 4. Note that bits 0-3 are duplicated: the control bits in these positions can only be written by the microcomputer, while the interface status bits can only be read.

MST and TRX

MST (master) controls the operation of the interface as a master or slave device:

MST = 1, master device

MST = 0, slave device.

TRX determines the direction of the data transfer:

TRX = 1, transmit data

TRX = 0, receive data.

Table 1 summarises the operating modes resulting from the four combinations of MST and TRX. A slave receiver is a device that receives both data and clock signals from a master transmitter. A slave transmitter is a device that

TABLE 1
Operating modes of the SIO interface

MST	TRX	MODE
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

has been addressed by a master transmitter, with a request to transmit data. The slave transmitter then transmits its data in accordance with the clock signal provided by the master receiver. (The master transmitter enters the master receiver mode to receive the data from the slave transmitter). A master transmitter is the only mode of operation in which a data transfer sequence can be initiated by the start conditions.

BB: Bus Busy

The Bus Busy flag indicates the status of the bus. Whenever a start condition is detected on the bus, the Bus Busy flag is set. It is reset by detection of a stop condition on the bus. In the master transmitter mode, the Bus Busy flag is used for the generation of start and stop conditions. Should a device attempt to generate a start condition while the flag is set, the Arbitration Lost (AL) flag will be set and a pending interrupt will be generated. The start condition will not be generated.

PIN: Pending Interrupt Not

PIN = 0 indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled. The pending interrupt is cancelled whenever data is read from or, written to, register S0. A pending interrupt is generated whenever a complete byte has been transmitted, the bus arbitration procedure is lost, a complete data byte is received or a valid device address is detected.

ESO: Enable Serial Output

The ESO flag enables/disables the SIO interface:

ESO = 1, the SIO interface is enabled

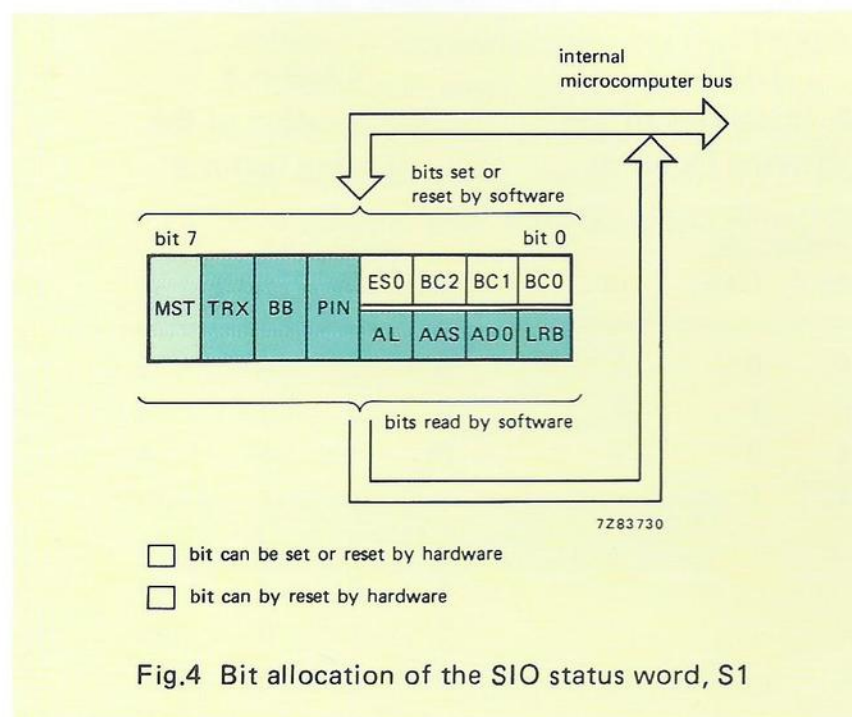
pin 2 is assigned the function of the serial data line.

ESO = 0, the SIO interface is disabled

pin 2 is assigned the function of I/O signal P23

the address register can be loaded by writing to S0.

ESO is set or reset by software but cannot be read.



BC0, BC1 and BC2

BC0, BC1 and BC2 form a counter for the number of bits in the byte to be received or transmitted. The counter can be set, but not read, by the microcomputer. The content of the counter indicates the number of bits/byte, with the exception that the value zero indicates an eight-bit byte. To eliminate the risk of spurious clock pulses affecting the counter while the bus is free, generation or reception of a start condition causes the counter to be reset. This has the result that the first byte of a transfer will always consist of eight bits.

AL: Arbitration Lost

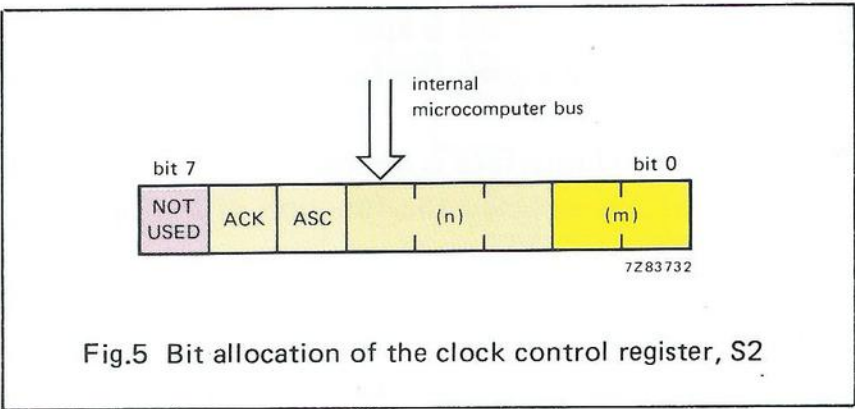
The Arbitration Lost flag is set by hardware when the SIO interface, as a master transmitter, loses a bus arbitration procedure. The interface then automatically enters the receiver mode to check if it is being addressed by the device that won the arbitration procedure. A pending interrupt will always be generated after reception of the byte during which arbitration was lost. When the microcomputer reads the status word, the Arbitration Lost flag will indicate that the required transmission did not take place. The Arbitration Lost flag will be reset when the pending interrupt is cleared (PIN = 1).

AAS: Addressed As Slave

The Addressed As Slave flag is set by hardware when the interface detects either its own specific address or the general call address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode. It is reset at the same time as the pending interrupt is cleared.

AD0: Address Zero

The Address Zero flag is set by hardware after detection of the general call address when the interface is operating in the address recognition mode. The general call address consists of a byte of eight zeros. The AD0 flag is reset when the bus becomes free after a stop condition.



LRB: Last Recieved Bit

This will contain either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Clock control register S2

Clock counter control

The five least bits of S2 are used to program the serial clock counter. The serial clock signal is derived from the internal clock of the microcomputer, which is one third of the frequency generated by the crystal clock circuit. When a 4.43 MHz crystal is used, the frequency of the serial clock may be programmed within the range 720 Hz to 100 kHz, using two dividing factors m and n. As can be seen in Fig.5, bits 0 and 1 are used to specify the required value of m according to Table 2, while bits 2, 3 and 4 are used to specify the value of n according to Table 3. The frequency of the serial clock signal can be determined from the equation.

fSCLK = fcrystal / (3 * m * n)

ACK: Acknowledge

For operation in the acknowledgement mode, both transmitter and receiver must have ACK = 1. The master device will then generate an extra clock pulse after each complete byte, as shown in Fig. 6. During the extra clock pulse, the transmitting device holds the data line High and the receiving device acknowledges by pulling the data line Low. The transmitting device stores the received acknowledgement signal in the LRB bit of S1.

TABLE 2
Specifications of the
dividing factor m

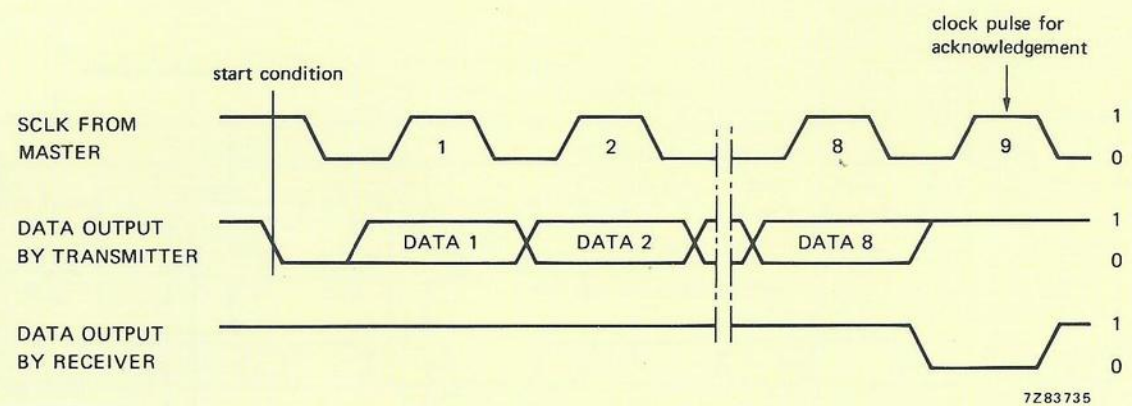
register S1		m
bit 1	bit 0	
0	0	5
0	1	6
1	0	7
1	1	8

TABLE 3
Specification of the
dividing factor n

register S1				n
bit 4	bit 3	bit 2	bit 1	
0	0	0	0	2
0	0	1	0	4
0	1	0	0	8
0	1	1	0	16
1	0	0	0	32
1	0	1	0	64
1	1	0	0	128
1	1	1	0	256

Archief
Ir. A.P.M. Moelands

Fig.6 Acknowledgement: an extra clock pulse is generated during which the receiver pulls the data line LOW



ASC: Asymmetrical Clock

ASC = 1 causes the clock generator to generate a serial clock with a Low to High ratio of 1:3. In this case, the dividing factor n must be 128, so that bits 4, 3 and 2 of S2 must be set to 1, 1, 0 respectively. The clock frequency is then given by the equation:

$$f_{\text{SCLK}} = \frac{f_{\text{crystal}}}{384m}$$

Address register

The address register contains the 7-bit address back-up latches and the ALS flag, as shown in Fig.7. The address latches hold the specific address allocated to the device, while the ALS (Always Selected) flag is used to enable/disable the address recognition mode.

ALS = 1, the SIO interface will respond to all messages, regardless of address.

ALS = 0, the SIO interface will respond only to messages containing its own address or the general address. In this mode, the least significant bit of the first byte received performs the function of read/write command (write = 0). When an interface detects its own address or the general call address, it automatically sets the TRX bit of the status word to the value of the received read/write command. The general call address (eight zeros) is thus a seven-zero address with the read/write command always zero.

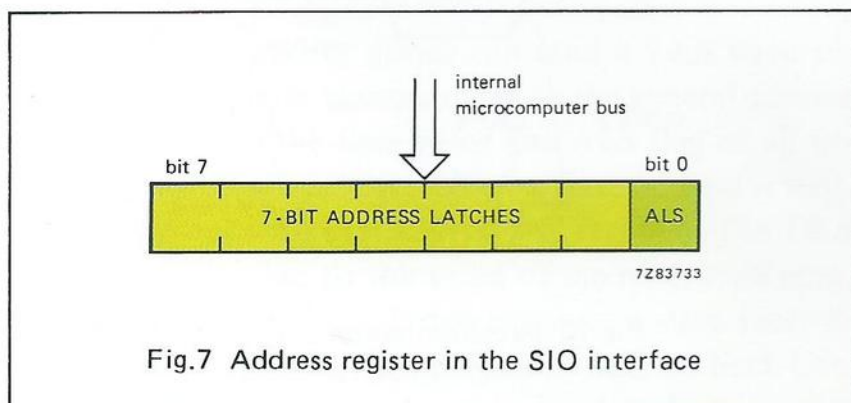


Fig.7 Address register in the SIO interface

The address register can only be loaded from the internal bus of the microcomputer when the SIO interface is disabled (ESO = 0). Under this condition, a MOV S0,A instruction will move the contents of the accumulator to the address register instead of S0, as would normally be the case.

Interrupt Logic

The interrupt logic can be enabled by an EN SI instruction, or disabled by a DIS SI instruction. When the logic is enabled, generation of a pending interrupt will result in a Serial I/O interrupt to the processor. An SIO interrupt causes the processor to execute the instruction at location 5 of its memory; the instruction is typically a jump to the beginning of the routine that handles SIO interrupts. When the logic is disabled, pending interrupts can still be serviced, as the PIN signal can be read from the SIO status word. However, the vectored interrupt will not occur.

Pending interrupts

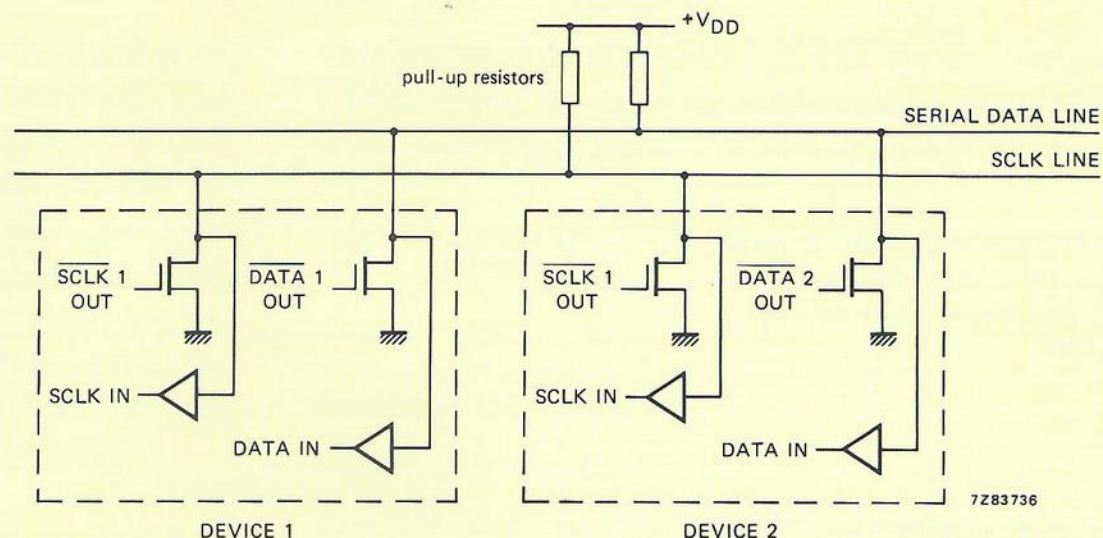
The first pending interrupt in a transfer sequence is generated when:

- a complete byte (data or address) has been transmitted
- the general call address is received
- the specific own address is received
- eight bits have been received and ALS = 1
- an arbitration procedure is lost and a complete byte is received.

Subsequent pending interrupts will be generated after the completion of each byte.

Once a pending interrupt has been generated, the clock line will be held Low until the interrupt is cancelled. This means that there will be a delay between bytes dependent on the interrupt processing time of the devices taking part in the transfer. Only when the clock line is released by all devices concerned, can transfer of the next byte be started.

Fig.8 Bus outputs have open drain configuration



Serial I/O operations

From the foregoing descriptions, it can be seen that once a device has generated a start condition, all Bus Busy flags in the system are set and no other device can initiate a transfer until the first device leaves the bus free. However, it is possible that two or more devices give a start condition almost simultaneously, so that none detects the start condition of the other(s). An arbitration procedure has therefore been designed into the interface so that only one device gets control of the bus.

Arbitration procedure

Figure 8 shows the open drain configuration of the serial bus outputs of the 8400 which gives the bus lines the wired AND property. This means that a Low level will overrule a High level on the line. The arbitration procedure uses the data presented on the serial data line by the competing transmitters. When a transmitter senses that a High signal it has presented on the line has been overruled by a Low signal, it switches to the slave receiver mode, sets the AL flag and generates a pending interrupt at the end of the byte. Figure 9 shows the arbitration procedure between two devices. The arbitration procedure will give priority to the device that transmits

the serial data stream with the lowest binary value. Should two or more devices send identical first bytes, arbitration will continue on the subsequent bytes. If the data streams are identical, an arbitration result is not necessary.

Clock synchronisation

Under normal conditions, only one master device will generate a clock signal. During the arbitration procedure, however, there are two or more master devices and the clocks must be synchronised so that the data outputs can be compared. The wired AND property of the clock line means that a device that first generates a low period of the clock line will overrule the other devices. At this High to Low transition, the clock generators of the other devices will be forced to start generation of their own Low period. The clock line will then be held Low by the device with the longest Low period, while the other devices that finish their low periods must wait for the clock line to be released before starting their High periods. A synchronised signal on the clock line is thus obtained, where the slowest device determines the length of the Low period and the fastest the length of the High period. An illustration of clock synchronisation is given in Fig. 10.

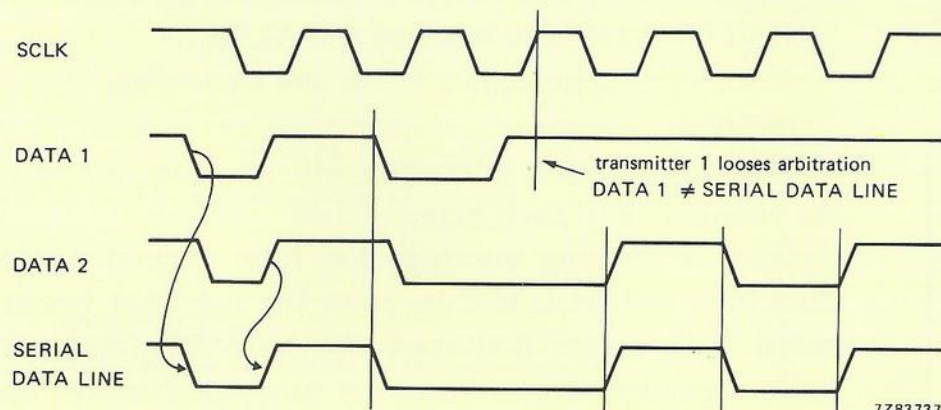


Fig.9 Arbitration procedure between two master transmitters

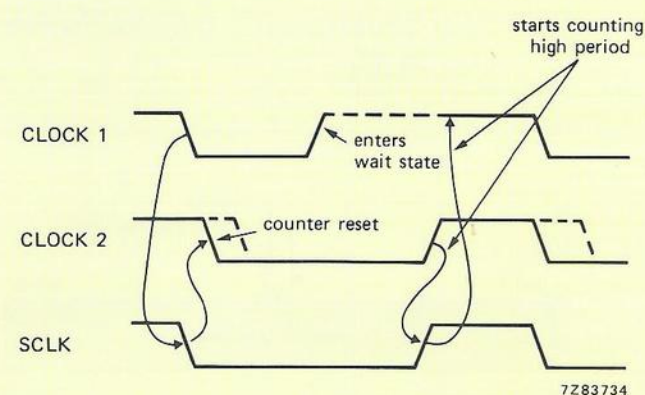
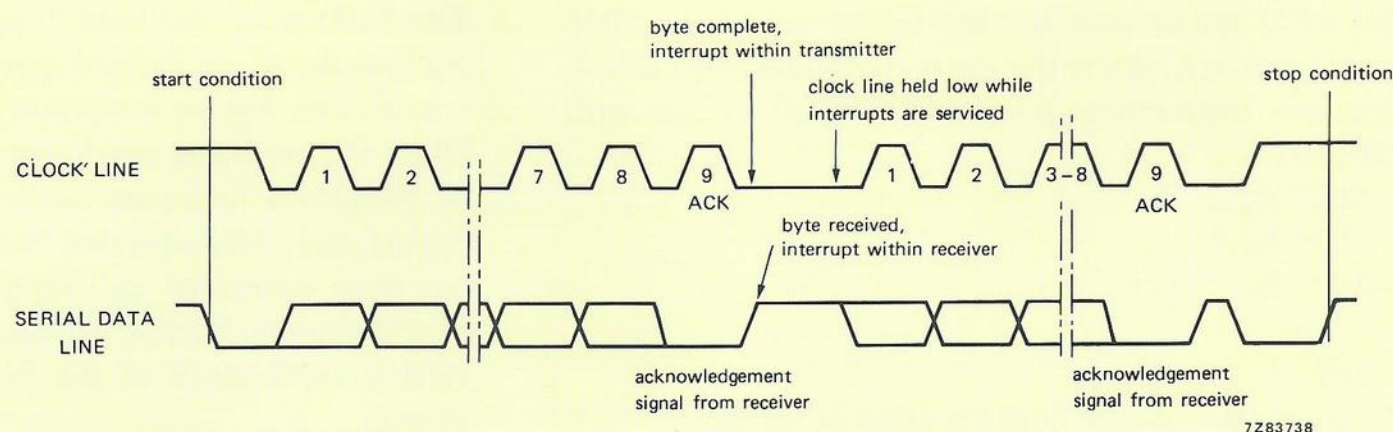


Fig.10 Synchronisation of clocks during the arbitration procedure

Fig.11 Transfer of two bytes without address recognition, in acknowledgement mode



Transfer modes

The 8400 SIO system has three basic transfer modes:

- transfer without address recognition
- transfer with address recognition
- transfer with asymmetrical clock.

Use of the acknowledgement procedure can be specified (ACK = 1 in both devices) with each of these three modes, giving a total of six options.

Transfer without address recognition

Transfer without address recognition is illustrated in Fig. 11. After reception or transmission of a complete byte, a pending interrupt will be generated, causing a serial interrupt request to the microcomputer if the interrupt logic is enabled. While the pending interrupt has not been serviced, the slave receiver will hold the clock line Low to indicate that it is not yet ready to continue with the subsequent data bytes. The receiver will service this interrupt by presetting the bit-counter in S1 and reading the data from S0. The transmitter will service the interrupt by presetting the bit-counter in S1 and writing data to S0. The pending interrupts are cancelled by the action of reading or writing data to or from S0. The transfer sequence is terminated by a stop condition from the master device, immediately following the last data byte.

Transfer with address recognition

In this mode, a master device can send a 7-bit slave address and read/write command bit or the general address of eight zeros as the first byte. The ALS flag of all devices should be set to zero. When a slave address is sent, only the device with that address will respond. The TRX bit of S1 will be set to the value of the read/write command bit such that the device becomes a slave receiver or a slave transmitter. The clock line will be held Low until the interrupts have been serviced in both master

and slave, after which data will be shifted into, or out of, the slave's shift register under control of the clock signal from the master device. When the master has addressed a slave with the command to transmit (least significant bit of byte = 1), the TRX bit in the master device will be reset so that the device enters the master receiver mode. After the first address byte any number of subsequent bytes may be transferred in the same way as described for transfer without address recognition.

When a general address is sent, all devices will enter the slave receiver mode and wait for data bytes from the master transmitter.

Transfer with asymmetrical clock

With a High to Low ratio of 3:1, the asymmetrical clock allows a microcomputer more time per clock period for sampling the data line, making the timing of this action less critical. Furthermore, because the clock line will often be used to generate interrupts, the reduced Low period will allow the microcomputer more processing time, as the microcomputer will be forced into the interrupt handling program all the time that the clock line is Low. Otherwise, the asymmetrical clock mode is the same as transfer without address recognition.

TABLE 4
8048 instructions not supported by the 8400 family

ANLD	P, A	—
CLR	F0	JNI
CLR	F1	MOVD A, P
CPL	F0	MOVD P, A
CPL	F1	MOVP3 A, @ A
ENTO	CLK	MOVX A, @ R
JF0		MOVX @ R, A
JF1		ORLD P, A

Instructions for serial I/O

The 8400 family uses the instruction set of the 8048 microcomputer, minus the instructions listed in Table 4. Five new instructions have been defined for use with serial I/O:

MOV A, S_n
 MOV S_n, A
 MOV S_n, # data
 EN SI
 DIS SI

Details of these instructions are given in Table 5.

Developments within the MAB 8400 series

The 8400 series has been designed for use in consumer equipment, where the reduction in the total number of connections has an important bearing on product cost. Other ICs are being developed to provide a useful range of peripheral functions, such as text-handling, display drivers and serial-operated memories. An inter-IC bus has been developed to simplify the use of these peripheral circuits. Further articles in the series will describe typical applications of the 8400 series and these peripherals.

TABLE 5
New instructions for serial I/O

mnemonic	op-code hex	bytes/ cycles	description of operation	function
MOV A, S _n	0C	1/2	Move contents of SIO register n to Accumulator	(A) – (S0)
	0D			(A) – (S1)
MOV S _n , A	3C	1/2	Move Accumulator contents to serial /IO register n	(S0) – (A)
	3D			(S1) – (A)
	3E			(S2) – (A)
MOV S _n , # data	9C	2/2	Move immediate data to serial I/O register n	(S0) – data
	9D			(S1) – data
	9E			(S2) – data
EN SI	85	1/1	Enable serial I/O interrupt	
DIS SI	95	1/1	Disable serial I/O interrupt	

Acknowledgement

The author wishes to thank Mr. H. Schutte and Dr. V. Timm for their contributions to this article.

Authors



H. J. H. van Heffen was born in The Hague in 1930 and joined Philips in 1949. While employed at the Research Laboratory he studied organic chemistry with the Royal Netherlands Chemical Society and Philips Technical Institute. In 1960 he transferred to the ceramics laboratory of the Electronic Components and Materials Division where, till 1970, he was engaged in the development of hard ferrites. Since then, as a member of the commercial department, he has been concerned with technical applications of magnetic ceramics.



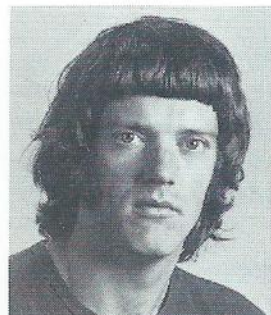
A. P. M. Moelands was born at Breda, The Netherlands, in 1951. After graduating in electrical engineering at the University of Technology, Eindhoven, in 1976, he joined the Central Application Laboratory of Philips' Elcoma Division. His work there on digital systems for television receivers led to an increasing concern with microcomputers and, eventually, to the development of the 8400 serial I/O described in this issue. He is now a member of the product marketing group *MOS microprocessors*.



Wim Rosink was born in Delden, the Netherlands, in September 1939. He studied electronic engineering at Enschede Polytechnic and received his Ing. degree there in 1959. After military service he joined the Central Application Laboratory of Elcoma, where he was first involved in the design of wideband amplifiers. In 1967 he became engaged in application work on devices for power control, especially for speed control of d.c. and a.c. motors. As a market application engineer based in Eindhoven he is now responsible for contacts with numerous European customers concerned with power control.



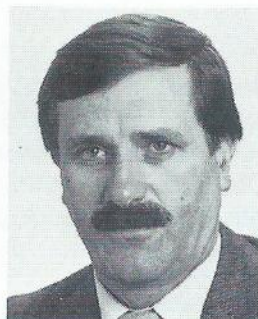
Peter R. Brennand studied at Imperial College, London, where in 1977 he gained a B.Sc. (Honours) in Electronic and Electrical Engineering. He then joined the Mullard Application Laboratory and worked initially on digital tuning systems for television. Since November 1979, he has been engaged in work on LSI frequency synthesiser systems for the professional market.



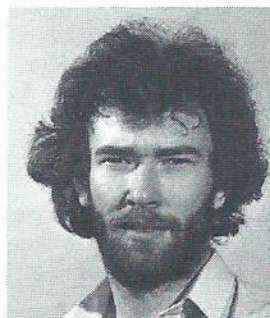
Ben H. A. Goddijn graduated in electrical engineering at the University of Technology, Delft, in 1973. In 1974 he joined Philips' Research Laboratories, Eindhoven, where he concerned himself with stepping motor design. In 1980 he gained his doctorate at the University of Technology, Eindhoven, with a dissertation on the stepping motor design described in this issue. He has recently moved to Philips, Drachten, where he is working on motors for small appliances.



A. A. J. Franken was born in Roosendaal, The Netherlands, in March 1941. He studied physics and electronics at the University of Amsterdam from 1959 and obtained a doctorate in 1965. Two years later he joined Philips, working in the Development and Application group of the Medical Systems Division, and specialised in X-ray image intensifier tv systems. Since 1976 he has worked in the Application Group, tv tubes, Elcoma.



W. Lohuis was born in Hilversum, the Netherlands in 1938. In 1960 he joined Philips' Research Laboratory, Eindhoven, where he was engaged in the development of photosensitive layers and pickup tubes. He completed his studies at the University of Technology, Eindhoven in 1964, and since 1968 he has worked in the Applications Group, tv pickup tubes, Elcoma.



Bruce Murray gained his B.Sc. (Honours) in Mathematics and Natural Philosophy at the University of Glasgow in 1978. Since then he has been attached to the Mullard Application Laboratory where he has been working on LSI frequency synthesiser systems for the professional market.

Archief
Ir. A.P.M. Moelands

Electronic components and materials

for professional, industrial
and consumer uses

from the world-wide
Philips Group of Companies



Argentina: FAPESA I.y.C., Av. Crovara 2550, Tablada, Prov. de BUENOS AIRES, Tel. 652-7438/7478.
Australia: PHILIPS INDUSTRIES HOLDINGS LTD., Elcoma Division, 67 Mars Road, LANE COVE, 2066, N.S.W., Tel. 427 08 88.
Austria: ÖSTERREICHISCHE PHILIPS BAUELEMENTE Industrie G.m.b.H., Triester Str. 64, A-1101 WIEN, Tel. 62 91 11.
Belgium: M.B.L.E., 80, rue des Deux Gares, B-1070 BRUXELLES, Tel. 523 00 00.
Brazil: IBRAPE, Caixa Postal 7383, Av. Brigadeiro Faria Lima, 1735 SAO PAULO, SP, Tel. (011) 211-2600.
Canada: PHILIPS ELECTRONICS LTD., Electron Devices Div., 601 Milner Ave., SCARBOROUGH, Ontario, M1B 1M8, Tel. 292-5161.
Chile: PHILIPS CHILENA S.A., Av. Santa Maria 0760, SANTIAGO, Tel. 39-40 01.
Colombia: SADAPE S.A., P.O. Box 9805, Calle 13, No. 51 + 39, BOGOTA D.E. 1., Tel. 600 600.
Denmark: MINIWATT A/S, Emdrupvej 115A, DK-2400 KØBENHAVN NV., Tel. (01) 69 16 22.
Finland: OY PHILIPS AB, Elcoma Division, Kaivokatu 8, SF-00100 HELSINKI 10, Tel. 1 72 71.
France: R.T.C. LA RADIOTECHNIQUE-COMPELEC, 130 Avenue Ledru Rollin, F-75540 PARIS 11, Tel. 355-44-99.
Germany: VALVO, UB Bauelemente der Philips G.m.b.H., Valvo Haus, Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040) 3296-1.
Greece: PHILIPS S.A. HELLENIQUE, Elcoma Division, 52, Av. Syngrou, ATHENS, Tel. 915 311.
Hong Kong: PHILIPS HONG KONG LTD., Elcoma Div., 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. 12-24 51 21.
India: PEICO ELECTRONICS & ELECTRICALS LTD., Ramon House, 169 Backbay Reclamation, BOMBAY 400020, Tel. 295144.
Indonesia: P.T. PHILIPS-RALIN ELECTRONICS, Elcoma Div., Panim Bank Building, 2nd Fl., Jl. Jend. Sudirman, P.O. Box 223, JAKARTA, Tel. 716 131.
Ireland: PHILIPS ELECTRICAL (IRELAND) LTD., Newstead, Clonskeagh, DUBLIN 14, Tel. 69 33 55.
Italy: PHILIPS S.p.A., Sezione Elcoma, Piazza IV Novembre 3, I-20124 MILANO, Tel. 2-6994.
Japan: NIHON PHILIPS CORP., Shuwa Shinagawa Bldg., 26-33 Takanawa 3-chome, Minato-ku, TOKYO (108), Tel. 448-5611.
(IC Products) SIGNETICS JAPAN, LTD, TOKYO, Tel. (03)230-1521.
Korea: PHILIPS ELECTRONICS (KOREA) LTD., Elcoma Div., Philips House, 260-199 Itaewon-dong, Yongsan-ku, C.P.O. Box 3680, SEOUL, Tel. 794-4202.
Malaysia: PHILIPS MALAYSIA SDN. BERHAD, Lot 2, Jalan 222, Section 14, Petaling Jaya, P.O.B. 2163, KUALA LUMPUR, Selangor, Tel. 77 44 11.
Mexico: ELECTRONICA S.A. de C.V., Varsovia No. 36, MEXICO 6, D.F., Tel. 533-11-80.
Netherlands: PHILIPS NEDERLAND B.V., Afd. Elonco, Boschdijk 525, 5600 PB EINDHOVEN, Tel. (040) 79 33 33.
New Zealand: PHILIPS ELECTRICAL IND. LTD., Elcoma Division, 2 Wagener Place, St. Lukes, AUCKLAND, Tel. 867 119.
Norway: NORSK A/S PHILIPS, Electronica, Sørkedalsveien 6, OSLO 3, Tel. 46 38 90.
Peru: CADESA, Rocca de Vergallo 247, LIMA 17, Tel. 62 85 99.
Philippines: PHILIPS INDUSTRIAL DEV. INC., 2246 Pasong Tamo, P.O. Box 911, Makati Comm. Centre, MAKATI-RIZAL 3116, Tel. 86-89-51 to 59.
Portugal: PHILIPS PORTUGESA S.A.R.L., Av. Eng. Duharte Pacheco 6, LISBOA 1, Tel. 68 31 21.
Singapore: PHILIPS PROJECT DEV. (Singapore) PTE LTD., Elcoma Div., Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. 25 38 811.
South Africa: EDAC (Pty.) Ltd., 3rd Floor Rainer House, Upper Railway Rd. & Ove St., New Doornfontein, JOHANNESBURG 2001, Tel. 614-2362/9.
Spain: COPRESA S.A., Balmes 22, BARCELONA 7, Tel. 301 63 12.
Sweden: A.B. ELCOMA, Lidingövägen 50, S-115 84 STOCKHOLM 27, Tel. 08/67 97 80.
Switzerland: PHILIPS A.G., Elcoma Dept., Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. 01/43 22 11.
Taiwan: PHILIPS TAIWAN LTD., 3rd Fl., San Min Building, 57-1, Chung Shan N. Rd, Section 2, P.O. Box 22978, TAIPEI, Tel. 5513101-5.
Thailand: PHILIPS ELECTRICAL CO. OF THAILAND LTD., 283 Silom Road, P.O. Box 961, BANGKOK, Tel. 233-6330-9.
Turkey: TÜRK PHILIPS TICARET A.S., EMET Department, Inonu Cad. No. 78-80, ISTANBUL, Tel. 43 59 10.
United Kingdom: MULLARD LTD., Mullard House, Torrington Place, LONDON WC1E 7HD, Tel. 01-580 6633.
United States: (Active devices & Materials) AMPEREX SALES CORP., Providence Pike, SLATERSVILLE, R.I. 02876, Tel. (401) 762-9000.
(Passive devices) MEPCO/ELECTRA INC., Columbia Rd., MORRISTOWN, N.J. 07960, Tel. (201) 539-2000.
(IC Products) SIGNETICS CORPORATION, 811 East Arques Avenue, SUNNYVALE, California 94086, Tel. (408) 739-7700.
Uruguay: LUZILECTRON S.A., Avda Rondeau 1576, piso 5, MONTEVIDEO, Tel. 91 43 21.
Venezuela: IND. VENEZOLANAS PHILIPS S.A., Elcoma Dept., A. Ppal de los Ruices, Edif. Centro Colgate, CARACAS, Tel. 36 05 11.