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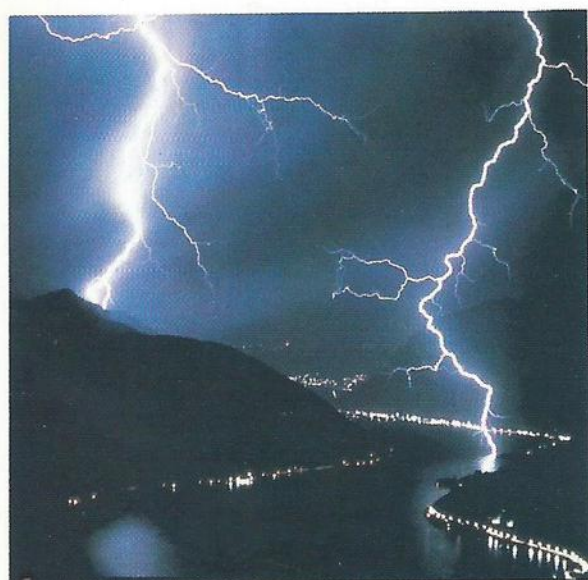
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Lightning, here striking the shore of Lake Lugano, is but one of the many hazards threatening the intricate telecommunications networks that knit today's global village together. While advances in solid-state have added greatly to what those networks can do, they have also increased their vulnerability. Safeguards that served in the days of electromechanical exchanges and rotary-dial, carbon-microphone subscriber sets are no longer adequate; the ICs in modern telephone systems are far more sensitive to excess voltages and currents. The article beginning on page 2 offers some useful suggestions about how to protect them against not only lightning-induced transients but other common hazards as well.

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When you need to exchange digital data between a number of sources and users, or over any distance, serial transfer may well be your best choice. Serial bus protocols and dedicated hardware to implement them now make it possible to extend digital techniques into many consumer and semi-professional application where the constraints of parallel transfer previously constituted a barrier.

Small area networks for serial data transfer

A. GOLDBERGER, C. KAPLINSKY, and A. P. M. MOELANDS

The attraction of serial data transfer is that it requires fewer lines — and, at least equally important, fewer line drivers, receivers, and signal-processing circuits — than parallel transfer. There are already many applications in which this is a decisive consideration, and with the inroads of digital electronics into homes, motor cars, and small businesses many more are in prospect.

Because microprocessors and microcomputers work with data in parallel form, parallel transfer is still the method of choice where distances are short and the number of devices sharing a communication channel is small. It is straightforward and fast, and in the disciplined environment of most computing and data-processing equipment the multiplicity of conductors required is unobjectionable. But in many other applications of digital data transfer that is not so.

The answer is then to sacrifice speed for simplicity and flexibility, and to opt for serial instead of parallel transfer. Two conductors are usually sufficient, and the additional requirement it imposes for parallel-to-serial and serial-to-parallel converters can be easily met by today's LSI.

SERIAL DATA LINKS

Figure 1 shows three types of serial data link.

A point-to-point link, joining only two stations, may be half-duplex, with transmission alternately in each direction, or full-duplex with transmission simultaneously in both directions. A loop network is a special type of point-to-point link in which data circulates in one direction only between a number of stations operating in half-duplex mode.

A multipoint network joins several stations; one is always the primary or master, controlling all transmission, and the

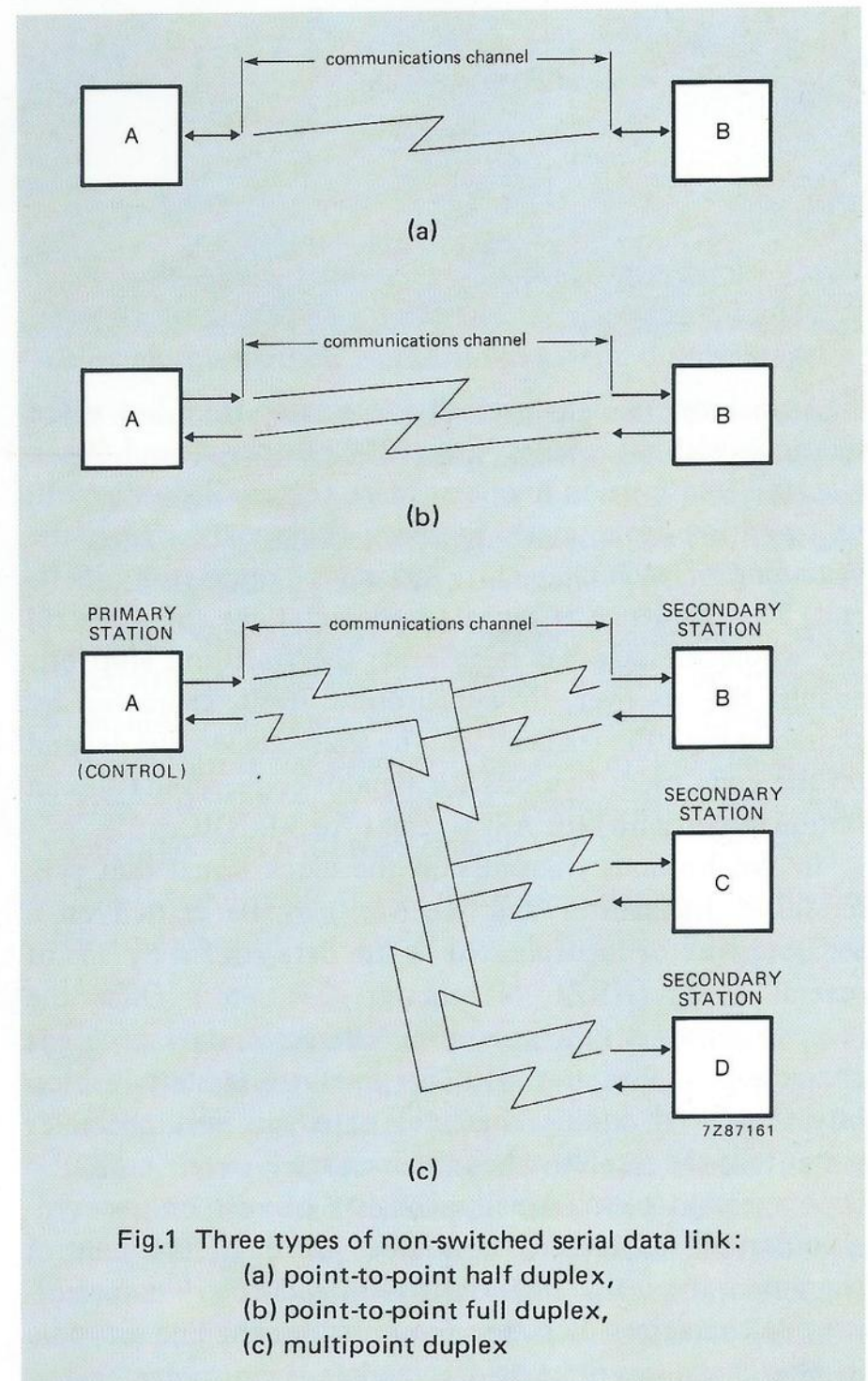


Fig.1 Three types of non-switched serial data link:
(a) point-to-point half duplex,
(b) point-to-point full duplex,
(c) multipoint duplex

others are secondaries. The stations may operate in half or full-duplex mode, and whenever transmission is in progress between the primary and one of the secondaries the others are idle.

Serial communication formats

Serial data can be transferred asynchronously (unclocked, Fig.2(a)) or synchronously (clocked, Fig.2(b)).

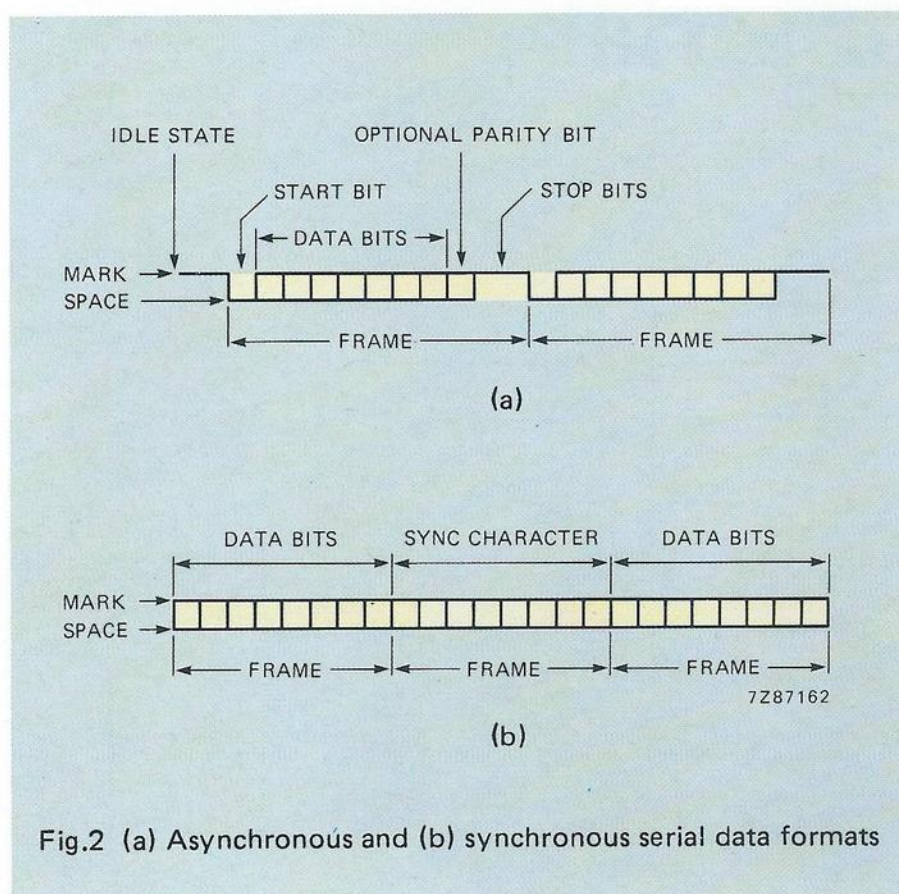


Fig.2 (a) Asynchronous and (b) synchronous serial data formats

Asynchronous data typically originates from low-speed terminals with rates of less than 1200 bits per second. When idle, the transmission line is at mark (binary 1); a start bit, or transition from mark to space (binary 0), signals the beginning of each character, and one or more stop bits its end. This sequence is repeated character by character till the whole message has been sent; the start and stop bits enable the receiver to synchronise itself character by character with the transmitter. The character lengths depend on the code used: five bits for Baudot code, seven (plus an optional parity bit) for ASCII, eight for EBCDIC.

In synchronous transmission the clock signal that synchronises transmitter and receiver may be carried on a separate wire or incorporated in the data stream by one of several codes (NRZI, Manchester, FM, etc.). Once the receiver senses a synchronisation character, data proceeds character by character with no intervening start or stop bits. A special ending character or a specified character count tells the receiver when the message is over.

A message block usually consists of one or two synchronisation characters, a number of data and control characters (typically 100 to 10 000), and one or two error-control characters. Between transmissions the line may idle in sync characters or be held at mark.

Asynchronous transmission is advantageous when the data flow is irregular, as from a keyboard operator's typing speed. Because of the simplicity of the interface logic and circuitry, it is also cheap. Synchronous transmission, on the other hand, makes far better use of the communication channel capacity by eliminating start and stop bits between characters. Furthermore, when using modems, it is suitable for multi-level modulation schemes which combine two or four bits in one signal element.

Protocols

To communicate with each other, all stations sharing a data link must of course use the same character code and the same syntax for assembling characters into messages; and to regulate traffic there must be a uniform set of control procedures, or protocols.

Data communication protocols break down into several levels, or layers, that define different types of function or operation. Each level is designed to be functionally independent of the others, but each depends on correct operation of the previous level. Protocol levels range from those that define the physical characteristics of the link (RS232C or CCITT V.35 for instance) to those responsible for functions such as message buffering, code conversion, fault recognition and reporting, communication with a host mainframe, and network management. The protocols are implemented by software packages such as IBM's Systems Network Architecture (SNA), CCITT's X.25, and DEC's DECnet.

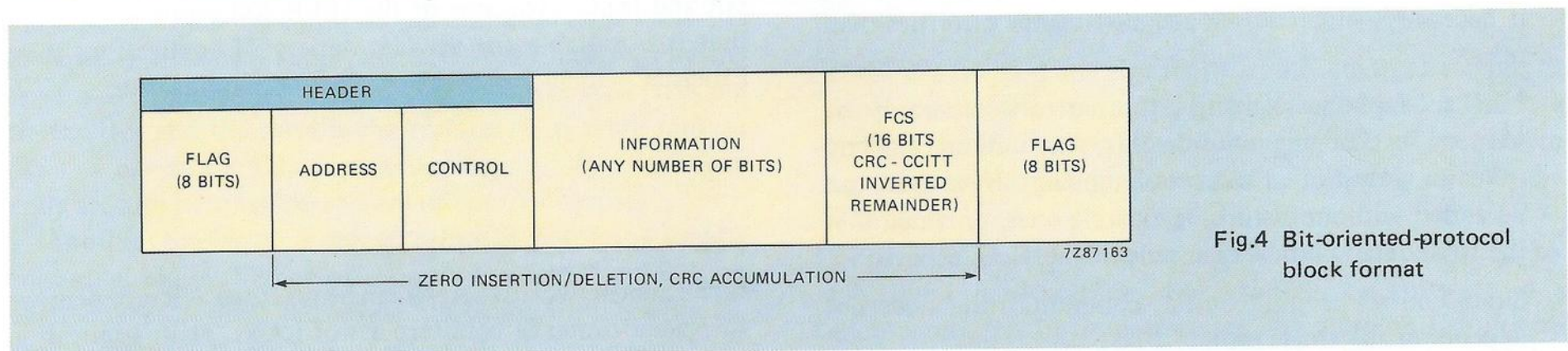
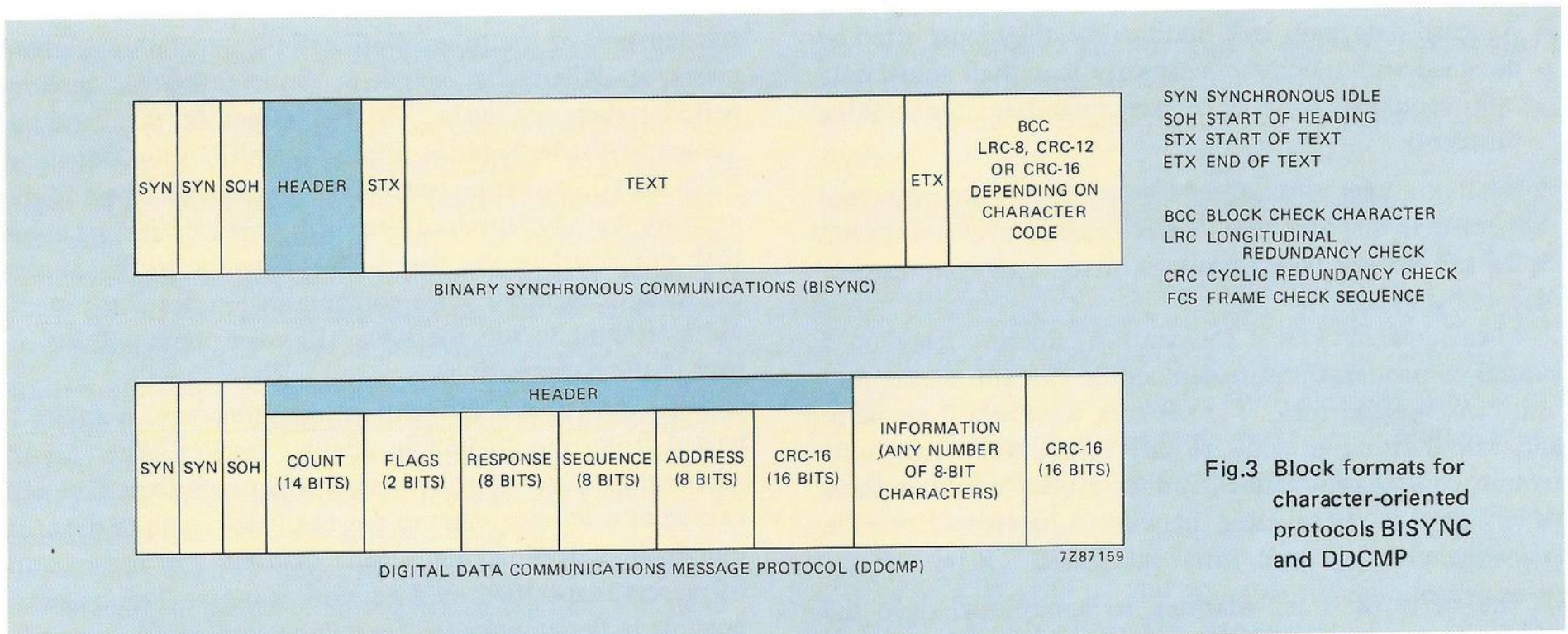
Data link control protocols (DLCs) are the sets of rules necessary to ensure effective communication between the stations sharing a link; their basic functions include

- making and breaking contact between two stations
- ensuring message integrity by error detection, requests for retransmission, and positive or negative acknowledgements
- identifying sender and receiver by polling or selection
- performing special control functions such as start and disconnect.

COPs and BOPs

Data link control protocols can be classed as character-oriented protocols (COPs) and bit-oriented protocols (BOPs).

In COPs a set of control characters forming part of an information code, such as ASCII or EBCDIC, governs the operation of the link. COP messages are transmitted in blocks consisting of a header or control field, a body or text field, and a trailer or error-checking field (Fig.3); special characters mark the block boundaries. Examples of COPs are IBM's Binary Synchronous Communication (BISYNC) and DEC's Digital Data Communications Message Protocol (DDCMP).



BOPs use only two or three control characters to govern operation of the link. These signal the beginning (FLAG) and end (FLAG, ABORT, GA) of a message frame. The fields comprising the bit sequence that follows the opening FLAG are transmitted in a set order of significance (Fig.4): address, control, text, and frame check. The lengths of the address, control, and frame-check fields are fixed; that of the text field is variable and may be zero. Examples of BOPs are ANSI's Advanced Data Communication Control Procedure (ADCCP), IBM's Synchronous Data Link Control (SDLC), ISO's High-Level Data Link Control (HDLC), and Burroughs Data Link Control (BDLC); the last three can be regarded as subsets of ADCCP.

LOCAL AREA NETWORKS

Local area networks (LANs) are more versatile than serial data links. Although the functional differences between the most advanced of the serial data links and the least advanced of the local area networks are small, there is nevertheless a fundamental distinction between them.

The essential characteristic of a serial data link is that it is autocratic; it relies on a master or primary station to control all communication on the link. Even if the data from one secondary station is meant not for the primary but for another secondary, the primary must first store the

data, poll the intended secondary to determine whether it is ready to accept the data, and then retransmit the data. Although this method works, it has several disadvantages:

- It does not adapt easily to changing conditions. If some stations have periods of peak activity, elaborate software algorithms must be written to take that into account. Moreover, if the system characteristics are ever changed, those algorithms have to be updated.
- It does not adapt easily to changing requirements. As all activity is centrally controlled, adding or removing secondary stations necessitates changing the software that controls the primary. This is so even if the secondaries affected need only to communicate with each other and not with the primary.
- The reliability of the entire system depends on that of the primary; if for any reason it fails, the entire system fails.
- If the system is one that relays control information to a decision-making centre, its data-gathering and status monitoring secondaries have to be polled continually. Often, however, the polling indicates no change and so returns little real information; thus, the overhead due to the polling protocol is high in relation to the data acquired. (This problem is dealt with differently in a computer. There, a peripheral unit takes the initiative and interrupts the computer when it requires attention.

As serial data links lack that facility, they must often be designed with much more capacity than their actual data rate requires, merely to accommodate the polling protocol).

These limitations of serial data links derive primarily from the fact that they are based on old electromechanical principles and do not take advantage of the opportunities now offered by VLSI.

Local area networks, by contrast, do not rely on a central controller; they are democratic, not autocratic. Any unit can take control of the network whenever it needs to and can transmit directly to any other. When two units require control simultaneously they arbitrate to determine which gets it. Local area networks therefore have the following advantages over serial data links:

- The network is self-adapting to conditions, since the attached units request to use it only when they need to; if necessary, some can be assigned higher priorities than others.
- Like a telephone exchange, the network can easily be adapted to changing requirements. Any unit can call any other or group of others (conferencing). New units can be added without disturbing existing ones, provided that the total data rate never exceeds the network capacity.
- Since control is not central, communication does not depend on any single unit.
- Since any unit can take control and address any other, the network in effect allows one unit to interrupt another. In a monitoring and control system, therefore, the network capacity need be scarcely larger than the required data capacity.

Local area networks are essentially electronic in character and do not rely on principles carried over from the electro-mechanical era.

Ethernet and IEEE 802

Local area networks already in use, or about to be, include Ethernet, Wangnet, Arcnet, and IEEE 802. Being intended for data rates of 10^6 to 10^7 bits per second over distances of 400 to 2000 metres, these are all overqualified for tasks such as transferring data between a terminal and a slow printer or between a floppy-disc file server and a terminal. They are well suited, however, to transferring data between two large computers with their own files or to carrying digitised voice communication as well as data. The latter application is one that typifies an important distinction between the two LANs currently enjoying the most support, Ethernet and IEEE 802.

In Ethernet any unit may seek access to the network whenever it detects no other activity on it. Since the propagation speed in the network is finite, however, it is possible for two units to test the network, find it idle, and start transmitting before either of them can detect the

transmission of the other. Both will then encounter garbled messages. When that happens, both retire for random periods, then try again. The net effect of this method, known as Carrier Sense Multiple Access/Collision Detection (CSMA/CD), is that no unit can be guaranteed access to the network for any length of time. Ethernet's detractors argue that this restricts the use of the network to few if any channels of digitised voice communication, for if too many units attempt to use the network, voice users will notice gaps in the conversation.

IEEE 802 uses a different access procedure. A token is passed from unit to unit in circular fashion. When a unit receives the token it either uses the network for a time not exceeding a set maximum or passes the token on to the next unit in line. The maximum time that any unit has to wait for access is specified by a network manager. This makes it possible to design units for a certain maximum data throughput and leads advocates of the IEEE 802 protocol to argue that it is suitable for a wider variety of applications than Ethernet — including digitised voice communication.

SMALL AREA NETWORKS

Small area networks (SANs) can be regarded as less expensive, lower-performance counterparts of LANs. Their application areas include

- the home, where they can be used to transfer control, information, and security signals
- business, where they can deal with traffic insufficient to justify a LAN or can serve as feeder networks to a LAN
- certain self-contained units, such as motor cars, where sensors, actuators, and services are necessarily remote from the operator's displays and controls.

Apart from size and performance, SANs differ from LANs in another important respect: LANs are big enough to justify professional managers to configure and administer them; SANs are not. A SAN should require no adaptation when units are added to the network or removed from it.

Two SANs that provide all the facilities of a LAN but on a much smaller scale have established themselves in the past two years, the Inter-IC bus (I^2C) and the Digital Data Bus (D^2B). Both are designed to cover only limited distances. The procedure for a unit attempting to use the bus is as follows:

- Wait until no activity is detected on the bus.
- Then issue a start bit which is unique and recognisable as such. (If a unit detects another's start bit just as it is about to issue one of its own, it retires and synchronises its internal clock on the edge of the detected start bit.)
- After the start bit, issue message bits serially, most significant bit first.

I²C and D²B are both wired-AND buses, which is essential to their method of resolving conflicts. Consider the situation when two units, A and B, happen to transmit simultaneously. Say A attempts to issue the signal 1101, and B the signal 1110. Both issue the first bit, a 1, and monitor the bus; both see a 1, so both proceed. The same occurs again on the second bit. But on the third bit A issues and sees a 0, while B issues a 1 and sees a 0 because of the wired-AND. This is a signal to B to retire immediately, as it has lost the arbitration. (The retirement must be immediate, otherwise a similar situation would occur again on the fourth bit, but in that case with A losing.) This method of arbitration works because the shortness of the bus sets a limit to the propagation time between any two units on it.

Besides using the same principle for arbitration, I²C and D²B are also similar in other respects. They both distinguish between master and slave and transmitter and receiver. The master is the unit that initiates an exchange with a slave. If it requests a slave to supply data, it is the receiver and the slave is the transmitter. If it supplies data to a slave, it is the transmitter and the slave is the receiver. Not every unit on the bus has to be able to function as a master; slave-only units are also permissible and are of course cheaper.

Another similarity is in the method of acknowledging correct receipt, whether of data or address. The line is an open collector one, and while the transmitter awaits acknowledgement it lets the line stay high. If the receiver does not pull it low within a prescribed time, the transmitter interprets that as a NACK (Negative ACKnowledge) indicating that what was sent was not correctly received. If a non-existent unit is addressed, the addresser will automatically see a NACK.

Apart from these similarities, I²C and D²B differ significantly in function, application area, and throughput characteristics.

I²C

The I²C bus is designed to provide the facilities of a local area network within a single system or equipment. It enables the system designer to distribute the system functions where they are most needed or convenient, without having to pay more than cursory attention to interconnection problems.

The bus consists of two lines, Serial Clock (SCL) and Serial Data (SDA), and, unlike other buses, permits more than one unit to drive the clock. This is possible because SCL is an open-collector line on which several units with their own internal clocks can operate together and synchronise with each other (Fig.5).

Normally, the SDA line changes only when SCL is low, so that the receiver can sample data on the rising edge of the next clock pulse. To generate a start condition however, SDA goes from high to low while SCL is high (Fig.6); this is a unique occurrence which enables all units to recognise the

start of a message. The stop bit is similarly unique: SDA goes from low to high while SCL is high.

A complete message on the I²C bus consists of the following fields:

START	SADD	R/W	ACK	DATA BYTE	ACK	STOP
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START Start condition (also called start bit)

SADD Slave address, a 7-bit field identifying the slave to be addressed and the priority of the message.

R/W Read/write, a single bit indicating whether the addressed slave is to be read from or written to.

ACK Acknowledge bit for the preceding field.

DATA A series of 8-bit characters, each followed by an ACK. There is not set limit to the number of characters in this field, although one may be imposed in certain implementations.

STOP Stop condition (also called stop bit).

There are no hard and fast limits to the length of the bus or the number of units that can be attached to it; there are implicit limits, however, due to the 400 pF maximum capacitance that can be connected to either the SCL or the SDA line.

The I²C bus can be monitored and driven either by specialised hardware or, more slowly, by software in a microcomputer. In the latter case, the start bit is followed by a start byte of the form 00000001 to give slaves which have the system algorithm implemented in software rather than hardware time to poll the data line. Once such a slave

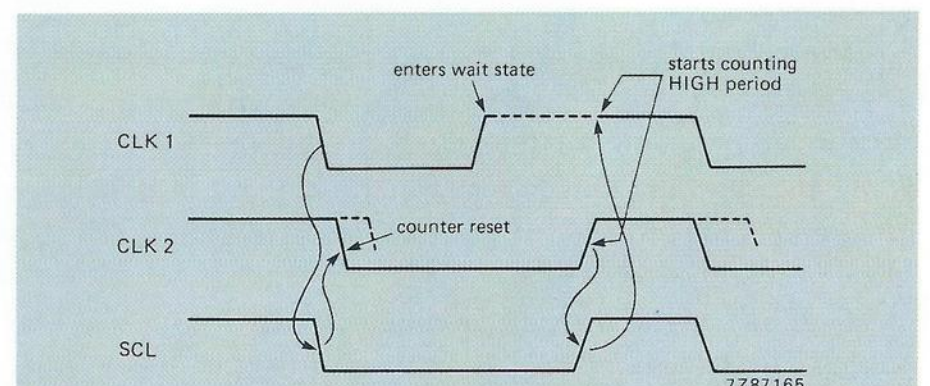


Fig.5 Clock synchronization on the I²C bus

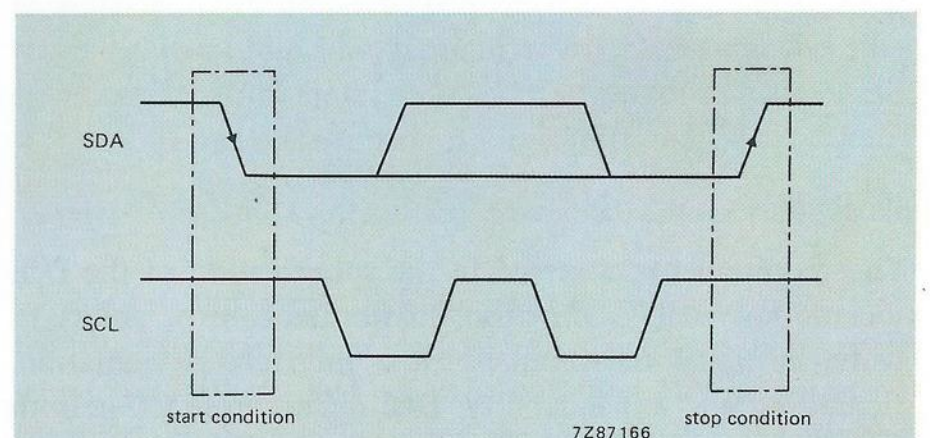


Fig.6 Start and stop conditions on the I²C bus

detects a low value on the SDA line, it switches to scanning the line more frequently.

The maximum bus throughput rate is 100 k bits per second, corresponding to about 11 k characters per second; lower rates can be achieved with slower devices making use of the clock synchronisation principle.

Typical applications of the I²C bus take advantage of the ease with which units can be added to or removed from it. As an example, consider the tv set illustrated in Fig.7. The 'standard' set includes the blocks on the right of the diagram. The control microprocessor has master capabilities and communicates with slave-only units in the keyboard, tuning control, tuning memory, and tuning display. The optional units on the left can be added or removed at any time; the ACK/NACK facility of the bus automatically tells the control microprocessor whether they are there or not.

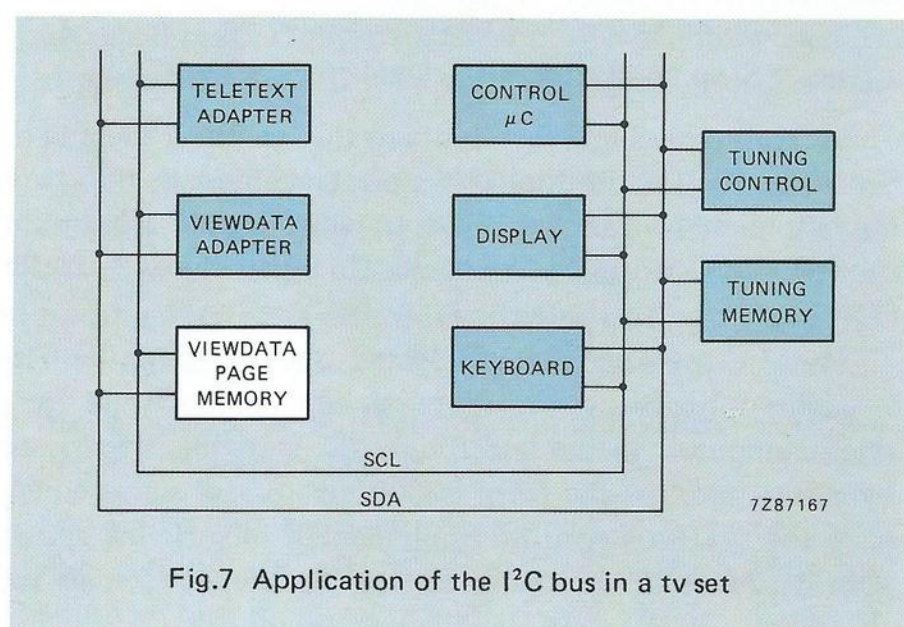


Fig.7 Application of the I²C bus in a tv set

The optional page memory for viewdata is an example of the ability to communicate on the bus without the controller even having to be aware of the unit's existence. Only the viewdata unit needs to communicate with the page memory, and, provided it has bus-master capability, it can do so directly.

The bus gives the set designer freedom to place the various units wherever is functionally best — the display and keyboard on the front panel, the tuning control away from heat sources, and the others where they can most easily be installed later as extras. It also gives him the freedom to redesign units to reduce cost, improve operation, or take advantage of new technology without worrying about the impact on other units in the system; only the two-wire interface and the command set need remain the same.

D²B

The requirements observed in the specification of the D²B include low cost, ease of use, distributed control, ability to work in noisy environment, low interference radiation, flexibility, and expandability. D²B differs from I²C in both protocol and method of transmission.

Part of the flexibility requirement is that units with different throughput rates must be able to share the bus.

Furthermore, low-throughput units should be less expensive to accommodate than high-throughput ones, and faster units should be switchable to slower speed for exchanging messages with slower ones. To meet these requirements the D²B has three operating modes, designated 0, 1 and 2 in ascending order of speed and cost.

Mode 0, the slowest, can be implemented by programming a microcomputer and providing suitable drivers and receivers. Mode 1 requires dedicated hardware but can work with a simple RC clock accurate to within 25%. Mode 2 requires a clock accurate to within 0.1%.

The bus can be up to 150 metres long and can accommodate as many as 50 units. All messages are limited to about 9 ms; in that time one data byte can be transferred in mode 0, 22 in mode 1, and 75 in mode 2. This corresponds to the following throughput rates if the bus is fully utilised and each transfer contains the maximum permissible number of data bytes:

	mode 0	mode 1	mode 2
bytes per second	110	≈2400	≈8200

These rates apply whether the bus is controlled continuously by one master or switched between several.

A message consists of the fields shown in Fig.8:

- A unique start bit to open the message and synchronise all units.
- One or more bits to identify the required operating mode. Mode arbitration works similarly to the address arbitration of the I²C; if two masters compete for the bus, the one using the lower mode prevails.
- Twelve bits to identify the address of the master and establish priority between competing masters. As the bus can accommodate only 50 units, the extra capacity of this field can be utilised to identify units as to type (f.m. tuner, VCR, amplifier, etc.).
- Twelve bits to identify the address of the slave.
- An acknowledge bit to confirm that the slave is on line and functioning.
- Four control bits to specify whether the transfer is to be a data, address* or status transfer, a read or a write, and whether the slave is to be locked onto a certain master.
- An acknowledge bit to confirm that the slave is able to perform the function required of it.
- One or more data bytes. Each character consists of 11 bits: the 8 data bits, a parity bit, an acknowledge bit, and an EOD (End Of Data) bit to show whether the message is over or more is to follow.

* Each unit on the bus can include a memory accessible to all the others which contains information on what the unit is and how to control it; i.e., a digital instruction manual. This information can be used by the interrogating unit and can also be transmitted in a form readable by the user of the system.

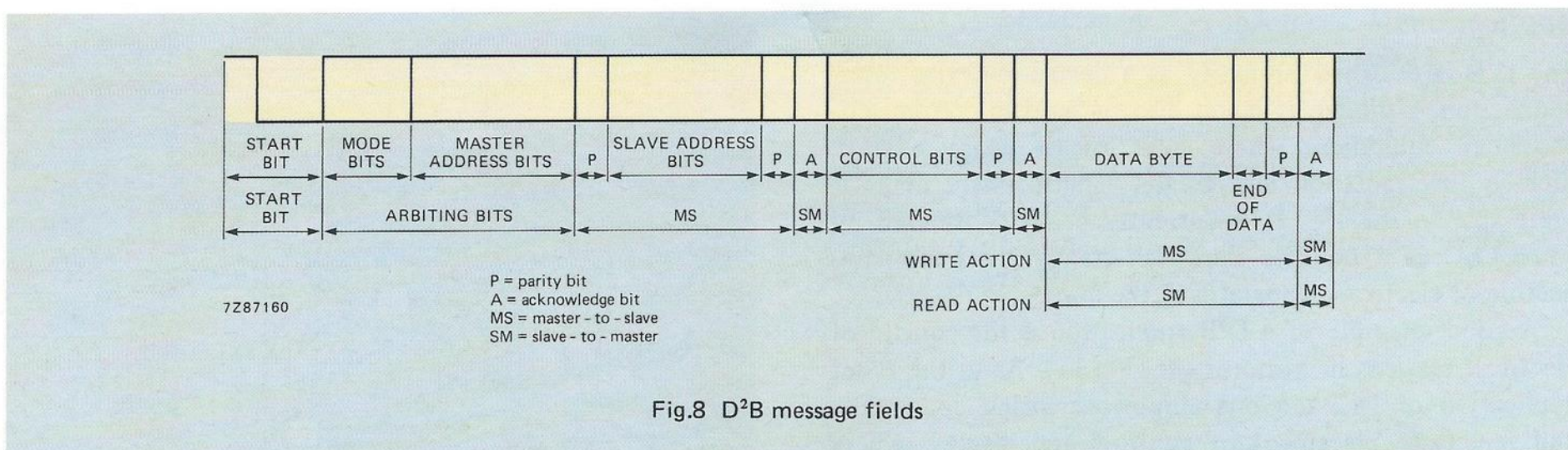


Fig.8 D²B message fields

Note that all except the start and mode-selection fields and acknowledge bits are followed by a parity bit.

The D²B uses only one line (actually a twisted pair, since signal transmission is differential) on which clock and data are time-division multiplexed. Each bit consists of the five parts shown in Fig.9:

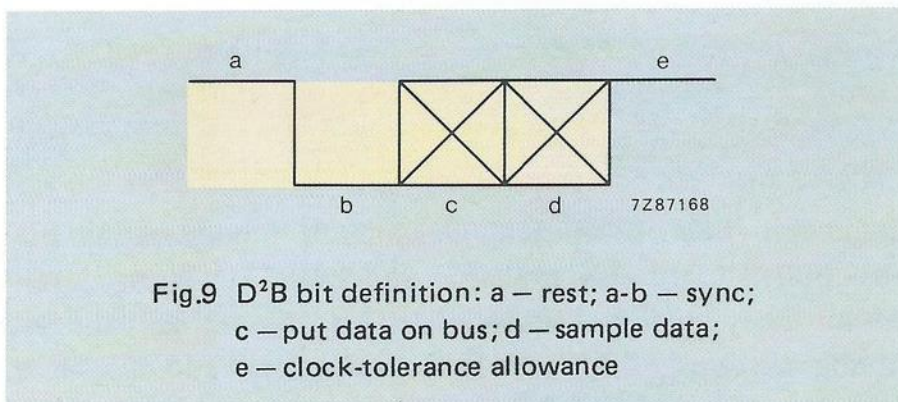


Fig.9 D²B bit definition: a — rest; a-b — sync;
c — put data on bus; d — sample data;
e — clock-tolerance allowance

- a — Rest time, to ensure that all units see a high level before the bus goes low.
- b — The high-to-low transition a-b is generated by the bus master and synchronises the clocks of all slave units.
- c — The time during which the transmitter puts data on the bus.
- d — The time during which the receiver samples the data.
- e — Allowance for unit-to-unit clock tolerances.

The specification of a bit in D²B, unlike that of most other systems, differs according to the function of the bit and takes account of all timing differences between units.

Timing

Consider Fig.10; by the time a square edge at the input of driver of unit A is clocked into unit B it will have been degraded by the following factors:

- the time through the driver of unit A
- the propagation time down the bus
- the RC rise or fall time
- the difference in clock phase between A and B
- the difference in clock frequency between A and B.

During an arbitration bit (mode or master-address field) unit A may generate the transition a-b (Fig.9), another unit may be putting data on the line (c), while a third may be sampling data (d). After the arbitration is completed only two units remain active on the bus and need be considered, the master and the slave.

The timing of a data transfer from master to slave is not the same as from slave to master. In a master-to-slave transfer the difference between the best and worst case in the master determines the timing. In a slave-to-master transfer the worst combinations of master and slave have to be taken into account, for the a-b transition that initiates each bit is always generated by the master.

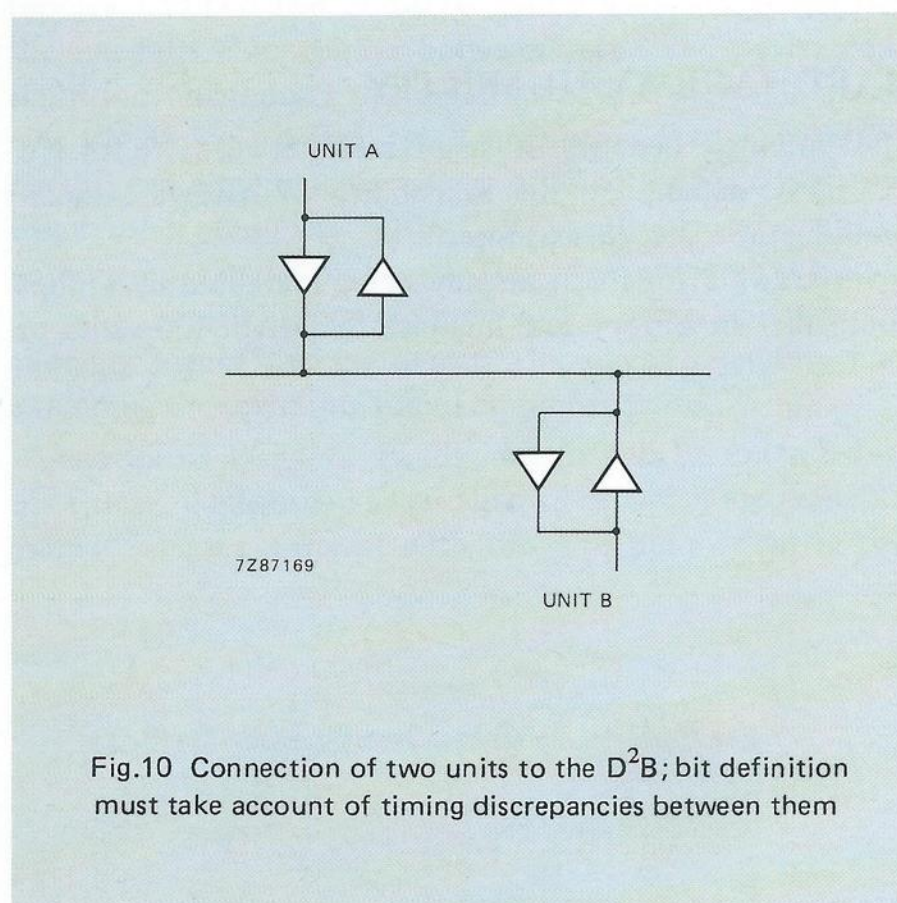


Fig.10 Connection of two units to the D²B; bit definition must take account of timing discrepancies between them

The bit timing specification must therefore be calculated for all combinations of master and slave: best/best, best/worst, worst/best, and worst/worst. The D²B is therefore specified at the bit level by the duration of the various phases of a bit, not only for the different message fields but also for the three operating modes.

Applications

The D²B is designed primarily as a device-to-device interconnection, although it could also be used in certain self-contained equipment where some of its characteristics, such as low radiation and greater length, might make it preferable to the I²C. It is currently being considered by CENELEC as a possible European standard for interconnection of electronic apparatus in the home.

A good example of a D²B application is the control of electrical services in a motor car (Fig.11). As in the tv-set application of I²C, the bus eliminates wiring constraints and facilitates placement of controls and displays where they are most convenient to the user. Master control panels within easy reach of the driver could control engine, entertainment, safety, comfort, and other services. Slave units at the sites of the services would decode the signals on the bus and perform the required functions. Options and extras would become easier to add; a power-controlled antenna, for example, could be installed without extensive rewiring. Diagnostic sensors could also be incorporated so that a computer connected to the bus could analyse such functions as ignition timing, carburetion or fuel injection, fuel consumption, combustion efficiency, lubrication efficiency, temperature control, and electrical system performance. It is conceivable that the widespread adoption of such a bus could lead to a fundamental reconsideration of many of the concepts that have dominated motor car design for most of the past century.

HARDWARE AVAILABILITY

The potential benefits of small area networks, both I²C and D²B, depend on the availability of hardware incorporating the bus logic and interfaces.

Hardware for I²C is already being marketed by Philips companies in Europe and includes the MAB8400 series of

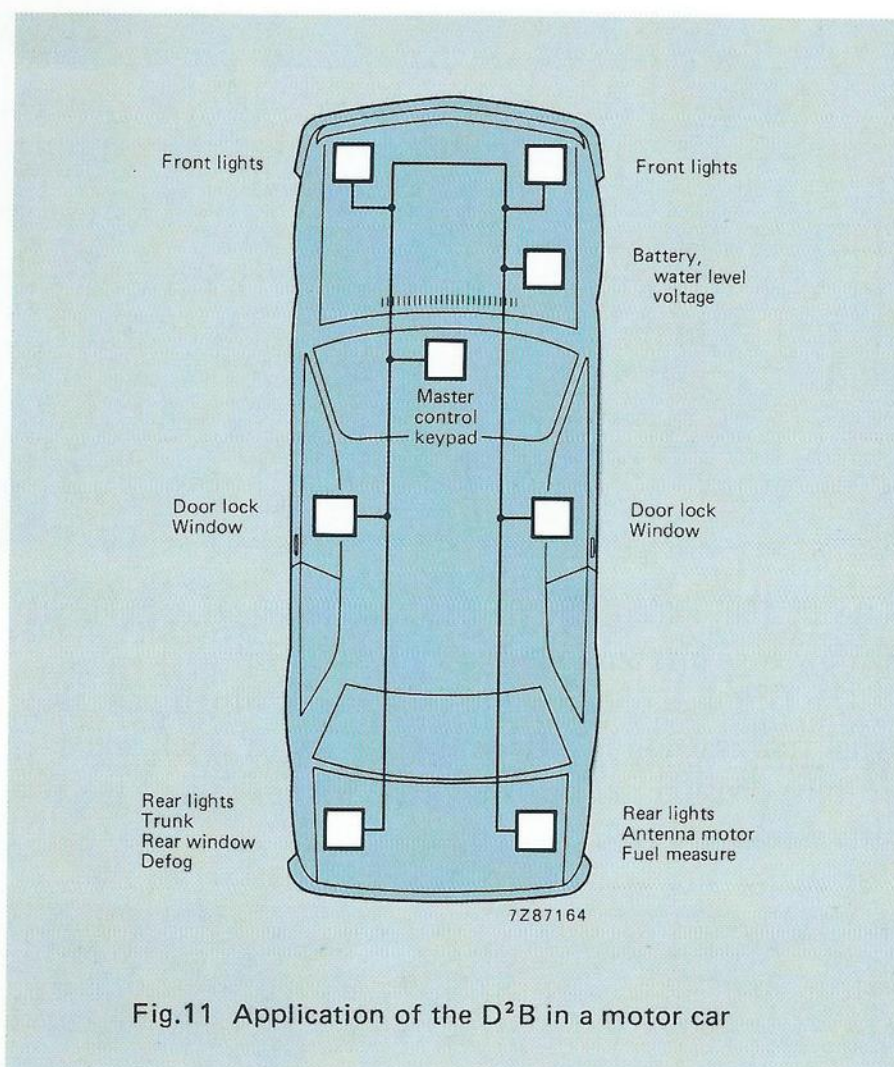


Fig.11 Application of the D²B in a motor car

single-chip microcomputers. Peripherals incorporating the bus interface are also available and more are being developed. They include display drivers, memories, timers, tuning systems, A/D and D/A converters, and a CMOS gate array for specialised functions.

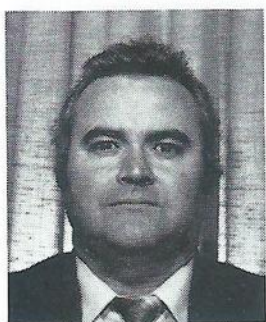
A recent licensing agreement between Philips, Signetics, and Intel will result in widespread availability in both Europe and North America of PCF80C48 and PCF80C51-based microcomputers incorporating the I²C and D²B buses, as well as development support products such as assemblers and in-circuit emulators.

ACKNOWLEDGEMENT

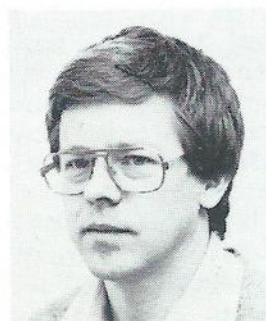
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Archief
Ir. A.P.M. Moelands

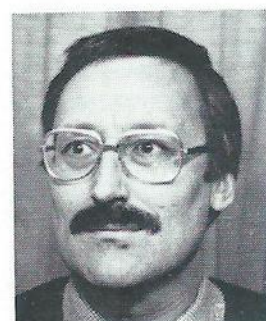
Authors



J.P. Coulmance, born in Neuilly, France, in 1944, graduated in electronics and, soon after, joined Sud Aviation where he worked on telemetry for the first French satellite launching. Later, he was engaged for about seven years in medical electronics development for Massiot Philips, and since 1974 he has been with RTC - La Radiotechnique-Compélec, in Paris, where he is now a member of the telecommunication group.



Rob Croes, born in Nijmegen, graduated in electrical engineering at 's Hertogenbosch in 1963. After military service he joined the IC development group of Philips Electronic Components and Materials Division, Nijmegen, where he worked on the design of bipolar digital ICs and is now involved in development of CMOS gate arrays and the new high-speed CMOS family.



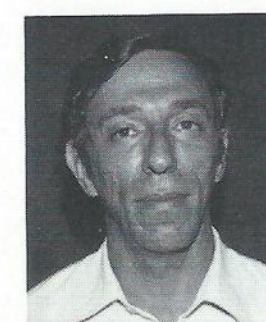
W. Eckert was born in Neusalz/Oder in 1943 and took his degree in electrical engineering in 1969. Since then he has been with Valvo, UB Bauelemente der Philips G.m.b.H., where he is now a member of the radio group of the application laboratory.



Alex Goldberger, who gained his MSEE at the Polytechnic Institute of Brooklyn, was design manager for the first large-scale integrated circuit for data communications. As applications manager for the microprocessor division of Signetics Corporation, Sunnyvale, he is responsible for application support, new product planning, and technical marketing support for microprocessor products.



J. Houthoff was born in Amsterdam, the Netherlands, in 1932 and graduated in mechanical engineering at the University of Technology, Amsterdam, in 1954. He joined Philips Electronic Components and Materials Division, Nijmegen, in 1960, initially working on diode and transistor development. Since 1965 he has been involved in the development of field-effect transistors.



Cecil Kaplinski took his M.Sc. in theoretical physics at the University of Cape Town in 1965. After ten years in various scientific posts at English universities, he joined Philips Data Systems, where he worked on operating systems. After that he worked on the application of software techniques to hardware design, initially at Philips Data Systems and Video divisions and now at Signetics.



J. C. F. van Loon was born at Tilburg, The Netherlands, in 1948. After studying electronic engineering at Philips' Technical School he joined the central application laboratory of the Philips Electronic Components and Materials Division where, as a member of the telephony group, he is engaged in design of electronic circuits for telephone apparatus.



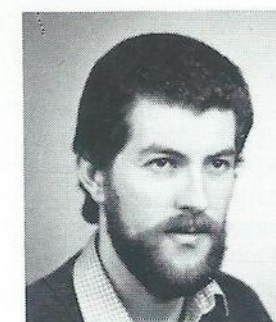
A. P. M. Moelands was born at Breda, The Netherlands, in 1951. After graduating in electrical engineering at the University of Technology, Eindhoven, in 1976, he joined Philips Electronic Components and Materials Division where he was instrumental in the development of the 8400 serial I/O. He is now a member of the product marketing group *MOS microprocessors*.



Frans Ohlenroth graduated in electronics at Amsterdam Polytechnic and, after military service as a radar specialist, joined Philips in 1960. During his career he has been responsible for the development of transmitting transistors and for international coordination of the semiconductor development laboratories of the Philips Electronic Components and Materials Division. He is now responsible for quality and reliability assurance in the bipolar IC group.



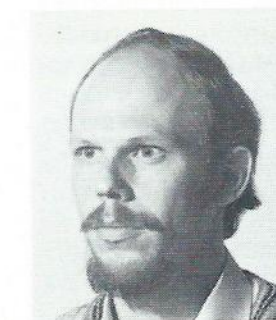
Lodewijk J. van Ruyven received his PhD in solid-state physics from the University of Technology, Eindhoven in 1964. After a period of postdoctoral research at the University of Delaware, he spent several years working at the Research Division of American Cyanamid. He joined Philips in 1969, and is currently head of Solid-State Laser Development, Philips Research Laboratories, Eindhoven.



Peter J. M. Sijbers joined Philips Electronic Components and Materials Division after graduating in electronic engineering at the Venlo Polytechnic. As a member of the central application laboratory he has worked on television tuners and i.f. integrated circuits and is now concerned with the design and application of ICs for telephone equipment.



T. H. Uittenbogaard was born in Wageningen, the Netherlands, in 1942. He joined Philips Electronic Components and Materials Division in 1961, initially working in the quality laboratory, electron tubes, and from 1963, at the u.h.f. tubes laboratory. Since 1965 he has been a member of the tv tuner group of the application laboratory at Nijmegen.



Jos Zeelen joined Philips Medical Systems Division in 1970 and, in 1974, moved to the central application laboratory of the Electronic Components and Materials Division, where he was a member of the radio group till 1982. Since then, as a member of the television group, he has been concerned with integrated circuits for i.f.

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