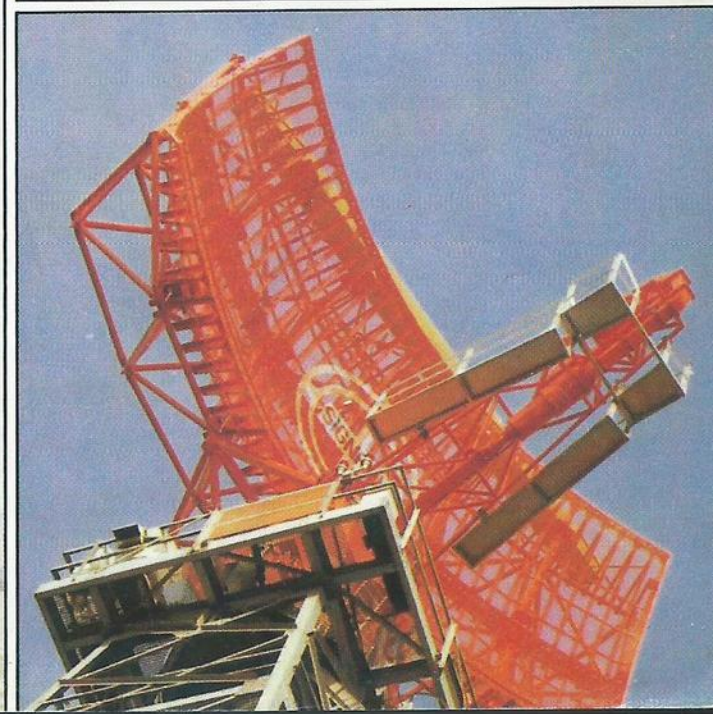
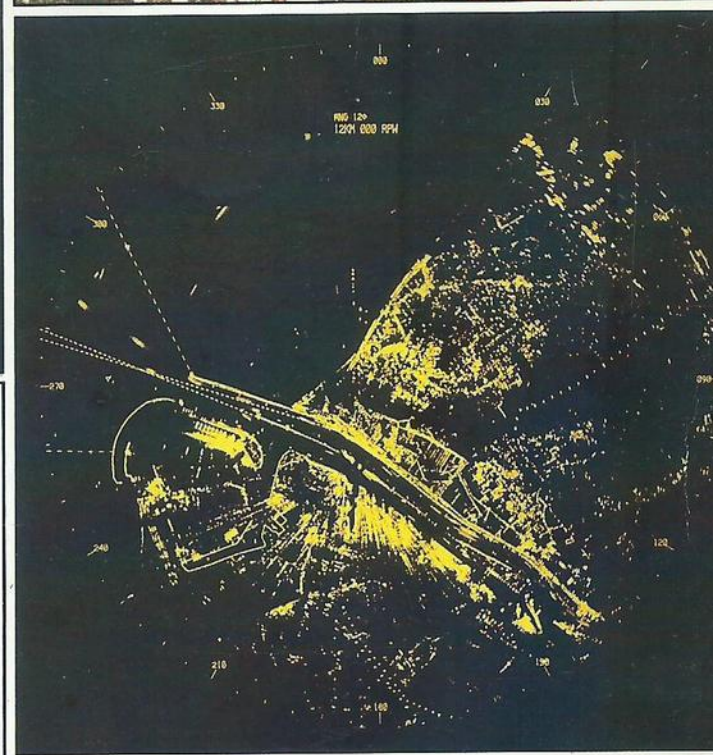
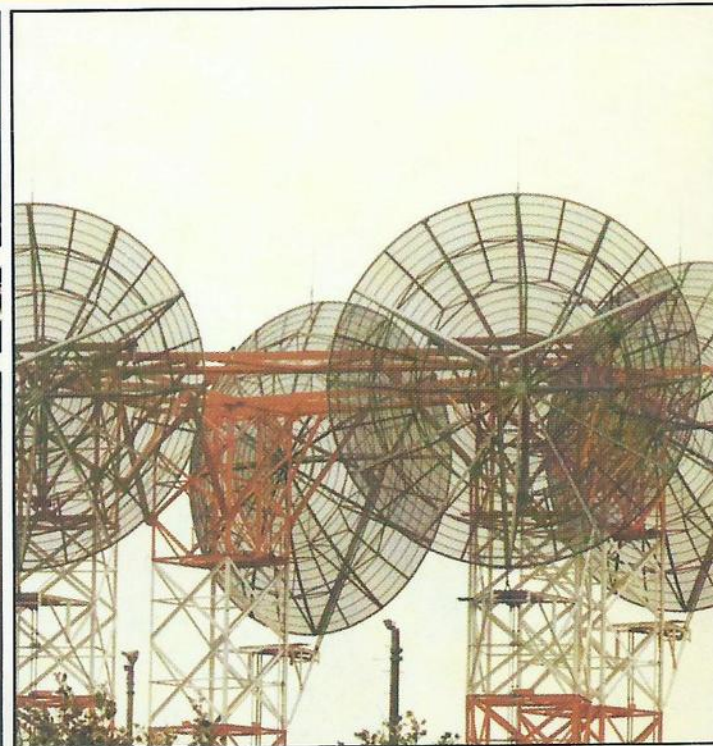


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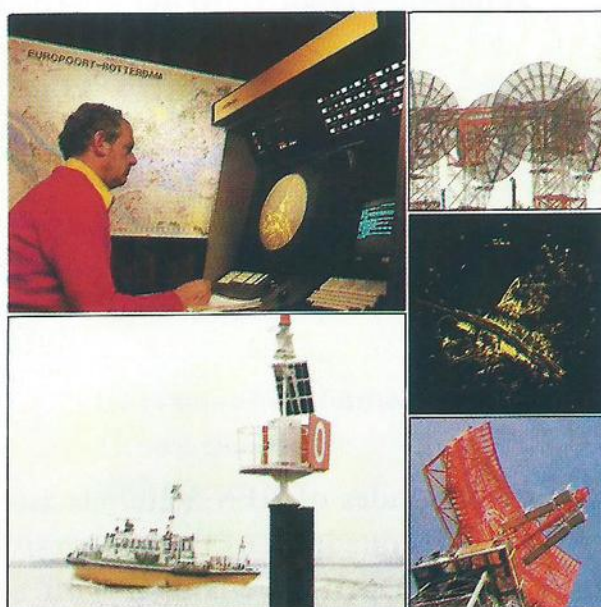
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Most important gateway to continental Europe, Rotterdam handles well over 30 000 ships a year — and with a safety record second to none. Nevertheless, the Vessel Traffic Management System which helps maintain this safety record is to be renewed. Work has already started on a new Traffic Centre, three of which will manage a new 26 station shore-based radar chain due for completion in 1986. Such very advanced projects, that must watch over the safety of ships and men and must protect the environment from many hazardous cargoes, call for reliability standards analogous to those of the aerospace industry. As major electronic component supplier, Elcoma has a proud record in meeting such standards.

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I²C bus in consumer applications

A. MOELANDS

Much of today's consumer-oriented electronic equipment contains at least one controller, usually a microcomputer, and a number of standard and dedicated integrated circuits for storing and displaying data, and for performing digital and analogue circuit functions. There are, of course, many ways of linking the internal circuit assemblies and interfacing the peripheral ICs with the microcomputer(s), but it's obviously of great benefit to equipment designers and manufacturers if the control interface is simple, standardised and facilitates equipment upgrading or conversion to unit construction. This is why we developed our Inter IC (I²C) bus and have included the hardware interface for it in a wide range of ICs for applications such as tv sets, video equipment, audio units, radios, telephones and automotive electronics.

The I²C bus is structured for economy, efficiency and versatility. Since data throughput for control functions is low, it transfers the control data serially in either direction at a rate of up to 100 kbits per second. This requires only two wires; one for the data and one for the system clock, so few IC pins and only simple print-board wiring and inter-board connectors are needed. Consequently, it doesn't limit the scale of integration per IC package and it reduces costs and board space. Furthermore, the I²C bus is a true multi-master bus so that control can be assumed by more than one of the ICs connected to it. To avoid loss or corruption of information, a unique address is allocated to each IC and the bus protocol incorporates an arbitration procedure to decide control priorities. When ICs with fast clocks communicate with others with slow ones, the protocol effectively synchronises the system clock by defining the clock source.

The I²C bus supports a wide range of microcomputers and peripheral ICs manufactured in many different semiconductor technologies and, since engineers and equipment manufacturers find it a powerful tool for system design and product development, it's fast becoming accepted as an industry standard.

BUS REQUIREMENTS

Serial Bus Information Transfer

The transfer of digital data within the equipment should be by way of a 2-wire serial bus which consists of a data line and a clock line. This decreases interconnection costs because printed-circuit boards are simplified and only two interconnection wires are required where functions are far apart as in modular equipment. For example, when the tuning function in a tv set is on the main pcb, and the control function and display is on the front panel. Connector costs for inter-board links are also reduced.

Another advantage of a 2-wire serial bus is that it only requires two pins on the IC. This leaves more pins available for achieving a greater degree of integration within each IC or allows package costs to be reduced by permitting the use of smaller packages.

Bidirectional Information Transfer

The serial bus must permit bidirectional data transfer. This requirement follows directly from the functional requirements of the system. For example, in a tv set, a non-volatile memory which contains the channel numbers or preferred analogue settings must be both read and written via the bus.

Binary Addressing of ICs

Modules or ICs must each have a unique binary address because there is no enable line in a two-wire system. This leaves more I/O available on the controller for other purposes.

Acknowledgement of Reception

The bus system must allow the receiving device to acknowledge reception of a message. This enables checks to be

made on the transfer of data and allows a master controller to determine the configuration of the system under control.

Multi-master Operation

It is essential for the bus system to allow multi-master operation. A master device is one that can initiate a data transfer. Multi-master operation allows more than one device to assume control of the bus to start a transfer. However, an arbitration system must be incorporated to ensure that information is not lost or corrupted when more than one master tries to simultaneously control the bus.

With multi-master operation there is no need for a central master (usually a microcomputer) to control all the functions. This means that incorporation of additional features or conversion of the system to a modular form will not affect the original system. The extra controls and software are contained within an additional master-controller which is simply clipped onto the bus.

Whereas with single-master operation the central controller has to transmit data continually, the controllers in a multi-master system need only transfer data of mutual importance. This reduces the data carried on the bus and allows the bus to be used more efficiently. In a multi-master system, with its inherent distributed intelligence, real-time interrupts can be handled locally and therefore, interrupts need not affect the whole system.

Multi-master operation also simplifies diagnostic procedures during which an additional master can be temporarily connected to the bus to implement programming or alignment routines.

Low-priced Slave Interface Implementation

Another important requirement is that the bus system must allow inexpensive hardware implementation of a slave interface. A slave is a device controlled by the current master.

The cost of the hardware interface to the bus is of paramount importance because it applies to each IC connected to the bus. For example, the interface should not require an internal oscillator in the slave because it would be redundant for many functions.

Standardised Protocol

The bus protocol must be standardised to allow a modular build-up of software.

THE I²C BUS

Definition of I²C bus terminology

Transmitter — The device which sends data to the bus

Receiver — The device which receives data from the bus

Master — The device which initiates a transfer, generates clock signals and terminates a transfer

Slave — The device addressed by a master

Multi-master — More than one master can attempt to control the bus at the same time without corrupting the message

Arbitration — Procedure to ensure that if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.

The I²C bus meets all the previously described requirements:

- It is a 2-wire serial bus consisting of a clock and a data line.
- It allows bidirectional data transfer.
- It is a real multi-master bus which means that more than one device capable of controlling the bus can be connected to it. Each master generates its own clock.
- Each IC has a unique 7-bit address and can operate as a receiver or transmitter.
- ICs can be considered as masters or slaves when performing data transfers.
- An arbitration procedure prevents corruption or loss of data when masters are competing for use of the bus.
- The first byte of a transfer contains the 7-bit slave address. The least significant bit of this byte is a direction bit.
- Every byte transferred is acknowledged by the receiver.
- The slave interface implementation is simple and inexpensive.
- The protocol is standardised.

Another feature of the I²C bus is that any master can operate the bus at its own speed as long as it does not exceed 100 kbits/s. Consequently the data transfers are asynchronous and the clock is only generated by each master as long as it is in control of the bus. If more than one master attempts to gain control of the bus simultaneously, a system clock signal is derived from the clocks of the active masters.

The input levels of the I²C bus have been designed with a view to protecting the ICs against line transients. For example, in a tv set, series resistors of up to 300 Ω can be used to protect the ICs against high voltage spikes on the data and clock lines due to flash-over of a television picture tube.

The maximum number of devices which can be driven from the bus is only limited by the maximum bus capacitance of 400 pF. The bus can therefore be up to 3 or 4 metres long.

General Characteristics

The serial data (SDA) and serial clock (SCL) lines are both bidirectional. Each is connected to a positive supply voltage via a pull-up resistor (see Fig. 1). When the bus is free, both lines are HIGH. The output stages of ICs connected to the bus must have an open-drain or open-collector to perform the wired-AND function. The number of ICs than can be connected to the bus, and its length, are solely limited by the maximum bus capacitance of 400 pF.

Due to the variety of different technology devices (CMOS, NMOS, bipolar) which can be connected to the I²C bus, the levels of the logical '0' (LOW) and '1' (HIGH) are not fixed but depend on the supply voltage of the ICs (see ELECTRICAL SPECIFICATIONS OF INPUT AND OUTPUTS OF I²C DEVICES). One clock pulse is generated for each data bit transferred. Data can be transferred at up to 100 kbits/s.

Data Validity

As shown in Fig.2, the data on the SDA line must be stable during the HIGH period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW (Fig. 2).

Start and Stop Conditions

As shown in Fig.3, a HIGH to LOW transition of the SDA line while SCL is HIGH indicates a start condition. A LOW to HIGH transition of the SDA line while SCL is HIGH is a stop condition. Start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition. The bus is considered to be free again a certain time after the stop condition. This bus free situation will be described later in detail.

Devices connected to the bus can easily detect start and stop conditions if they possess the necessary interfacing hardware. However, microcomputers with no such interface have to sample the SDA line at least twice per clock period to sense the transitions.

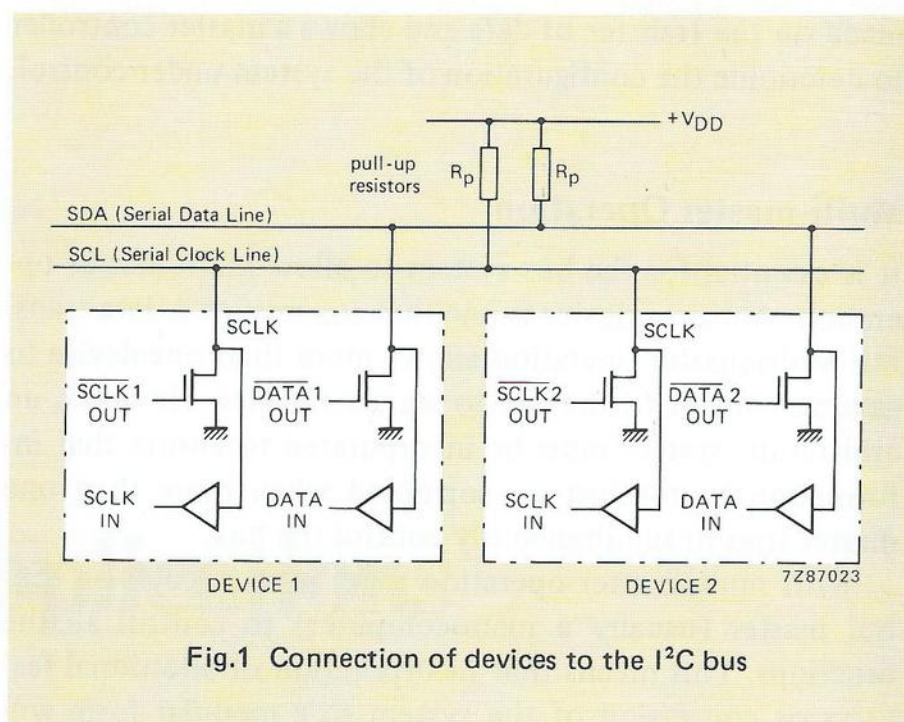


Fig.1 Connection of devices to the I²C bus

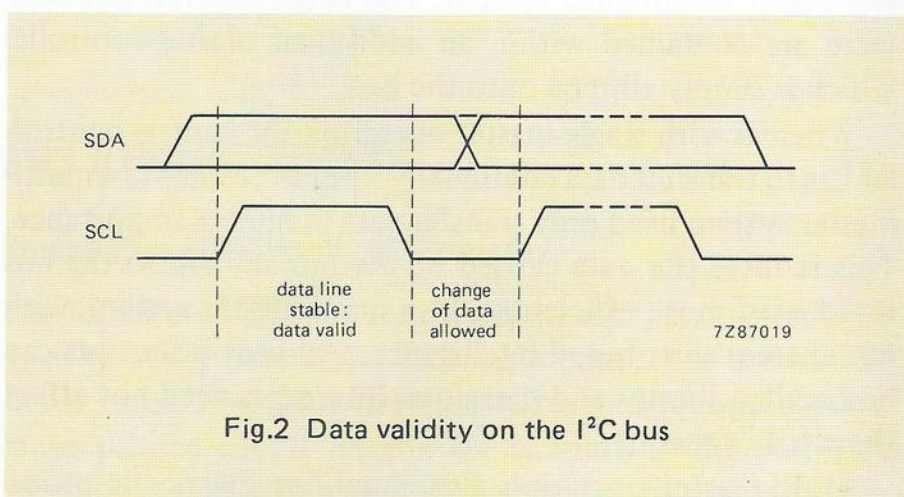


Fig.2 Data validity on the I²C bus

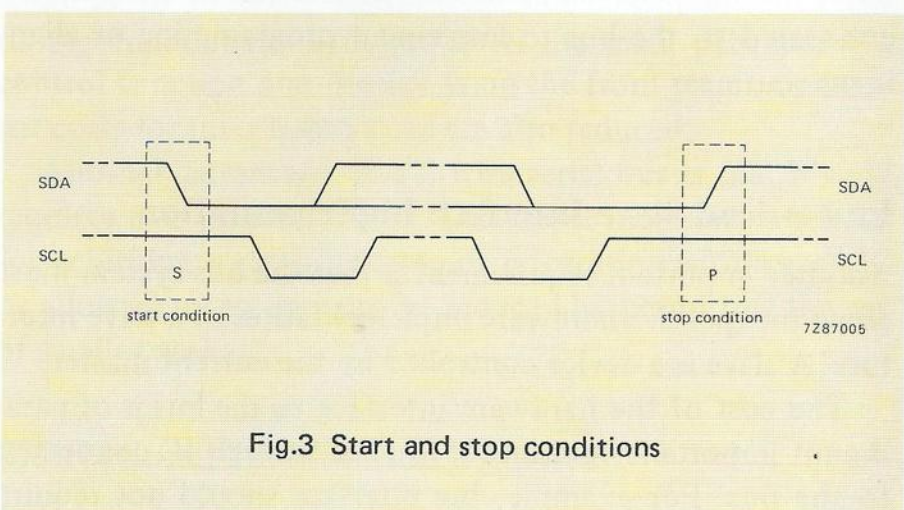


Fig.3 Start and stop conditions

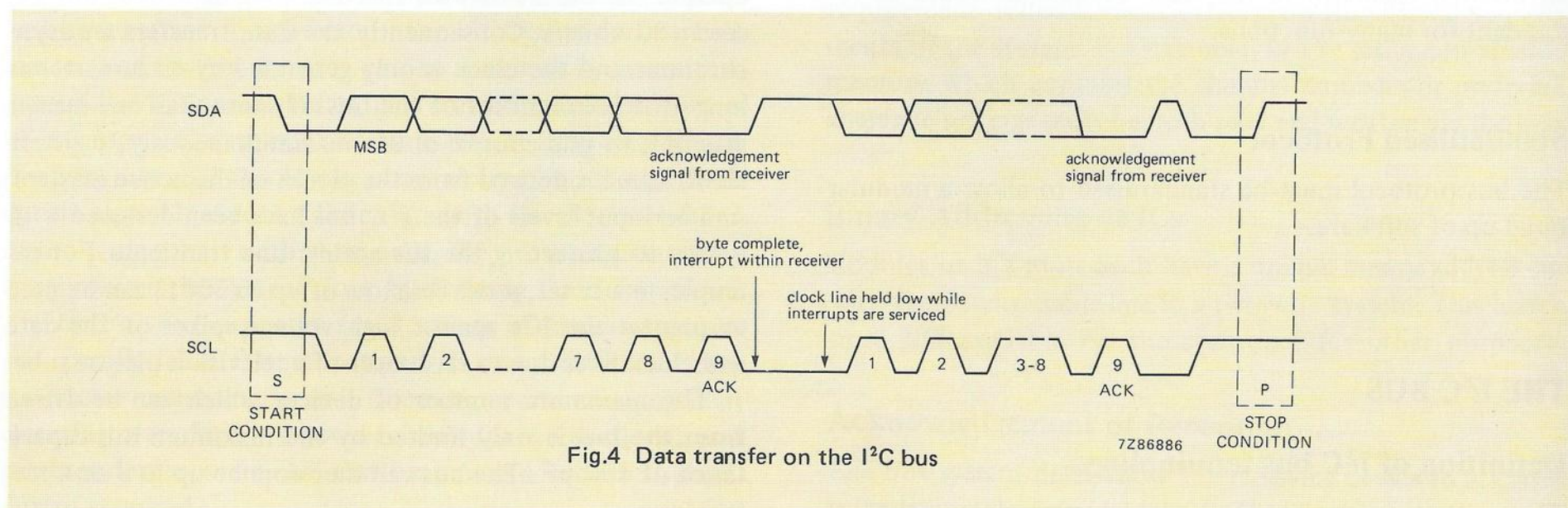


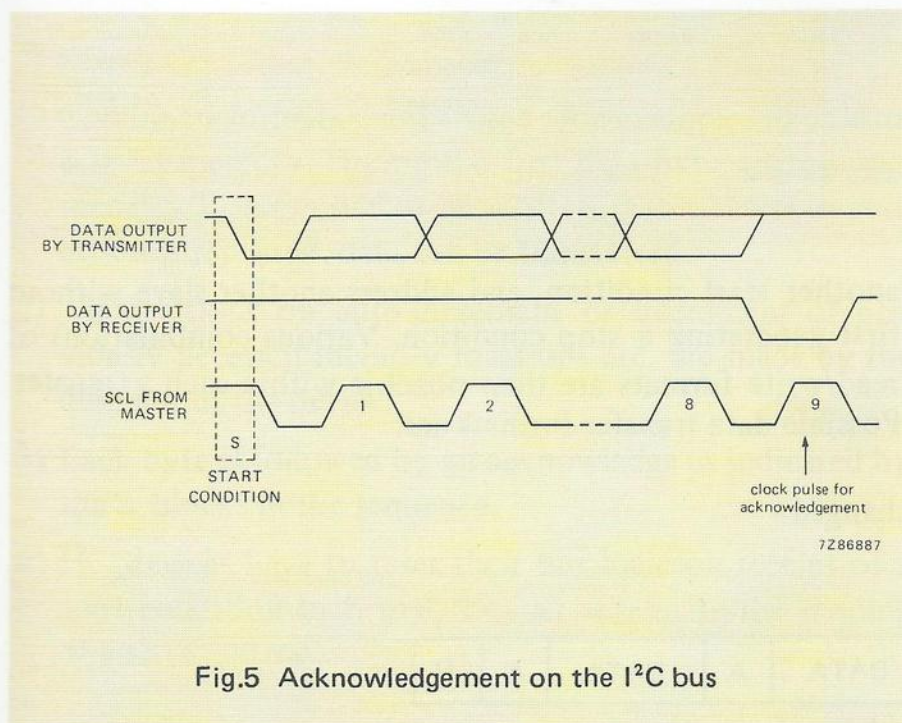
Fig.4 Data transfer on the I²C bus

Transferring Data

Byte Format. Every byte transferred on the SDA line must contain 8-bits. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge bit. As shown in Fig. 4, the most significant bit (MSB) is transferred first. If a receiving device cannot receive another complete byte of data until it has performed some other function, for example, serviced an internal interrupt, it can hold clock line SCL LOW to force the transmitter into a wait state. Transfer then continues when the receiver is ready for another byte and releases clock line SCL.

Acknowledge. The acknowledge-related clock pulse is generated by the current master. The transmitting device releases the SDA line (HIGH) during the acknowledge clock pulse. The receiving device must pull down the SDA line (LOW) during the acknowledge clock pulse so that the SDA line is stable LOW during this clock pulse (Fig. 5). Of course, set-up and hold times must also be taken into account. A receiver which has been addressed is usually obliged to generate an acknowledge after each byte has been received. When a slave receiver does not acknowledge its address, for example if it is not able to receive because it is performing some real-time function, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer.

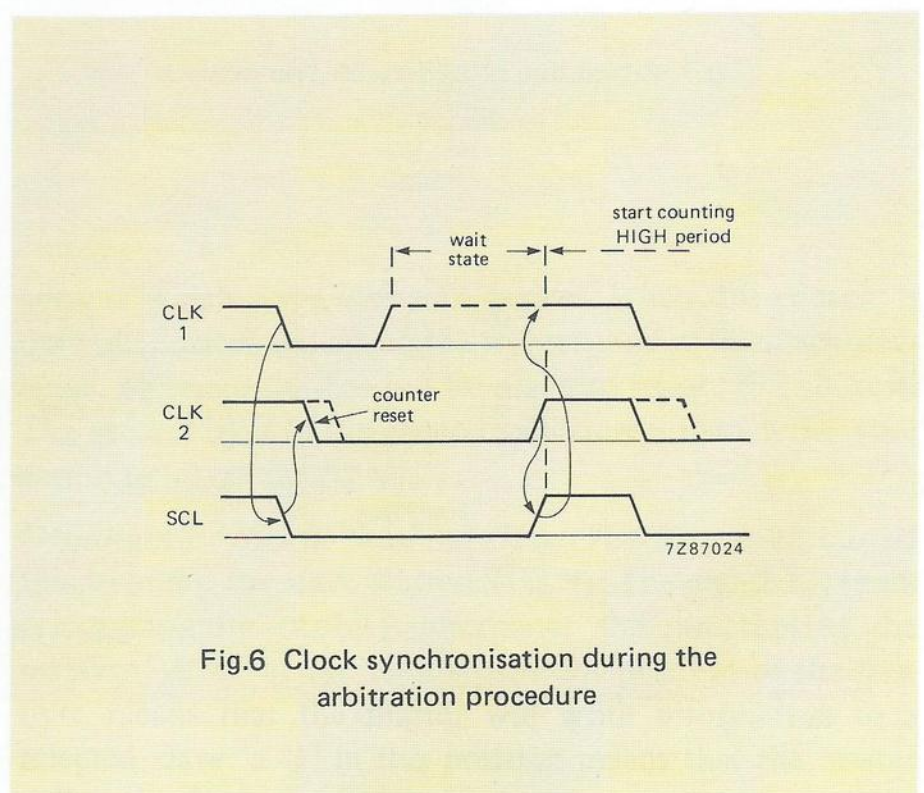
If a slave receiver acknowledges its slave address, but some time later in the transfer cannot receive further data bytes, the master must again abort the transfer. This is indicated by the slave not acknowledging a data byte by leaving the data line HIGH. The master then generates the STOP condition.



If a master receiver is involved in a transfer, it must signal an end of data to the slave transmitter by not acknowledging the last byte from the slave transmitter. The slave transmitter must then release the data line to allow the master receiver to generate the stop condition.

Clock Generation and Arbitration

Synchronisation. All masters generate their own clock on the SCL line during transfer of data. Data is only valid during the clock HIGH period. A defined clock is therefore needed to allow the bit-by-bit arbitration procedure to take place. Clock synchronisation is performed using the wired-AND connection of devices to the SCL LINE. As shown in Fig. 6, a HIGH to LOW transistion on the SCL line causes all competing devices to count off their LOW periods and the SCL line is held low until the device with the longest LOW period finishes its count. Devices with shorter LOW periods remain in a HIGH wait state during this time. When all devices concerned have counted off their LOW periods, the clock line is released and goes HIGH. There is then no difference between the state of the device clocks and the state of the SCL line, and all devices start counting their HIGH periods. The first device to complete its HIGH period count pulls the SCL line LOW. In this way, a synchronised SCL clock is generated, the LOW period of which is determined by the device with the longest clock LOW period and the HIGH period of which is determined by the device with the shortest clock HIGH period.



Arbitration. Arbitration ensures that a master which transmits a HIGH level on the SDA line while another master transmits a LOW level, will switch off its DATA output stage because the level on the bus does not correspond to its own level. Arbitration can continue during many bits. The first stage of arbitration is the comparison of the address bits. If the masters are addressing the same device, arbitration compares the data bits. Because address and data information is used for the arbitration, it does not delay the transfer of information.

A master which loses the arbitration can generate clock pulses until the end of the byte in which it lost the arbitration. If a master loses arbitration during the addressing procedure, it is possible that the winning master is trying to

address it. The losing master must therefore switch over immediately to its slave receiver mode.

Figure 7 shows the arbitration procedure for two masters. Of course more masters may be involved. As soon as the master generating DATA 1 generates an internal HIGH level whilst the data on the SDA line is LOW, it switches its output off so that the master generating DATA 2 wins the arbitration and its output continues to be transferred on the SDA line. Since arbitrations are decided solely on the basis of addresses and data transmitted by competing masters, there is no central master, or any order of priority on the bus.

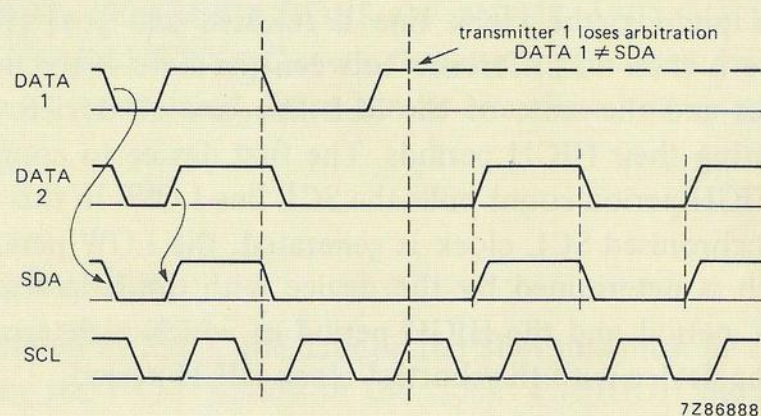


Fig.7 Arbitration procedure for two masters

Use of the Clock Synchronising Mechanism as a Handshake. In addition to being used during the arbitration procedure, the clock synchronisation mechanism can be used to enable receiving devices to cope with fast data transfers, either on a byte or bit level.

On the byte level, a device may be able to receive data bytes at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slave devices can then hold the SCL line LOW, after reception and acknowledgement of a byte, to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

On the bit level, a device such as a microcomputer without a hardware I²C interface on-chip can slow down the bus clock by extending each clock LOW period. In this way, the speed of any master is adapted to the internal operating rate of this device.

Formats

The data transfer format is shown in Fig. 8. After the start condition, a 7-bit slave address is transmitted and followed by a data direction bit ($R/\bar{W}$); a '0' indicates WRITE, a '1' indicates READ. A data transfer is always terminated by a stop condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate

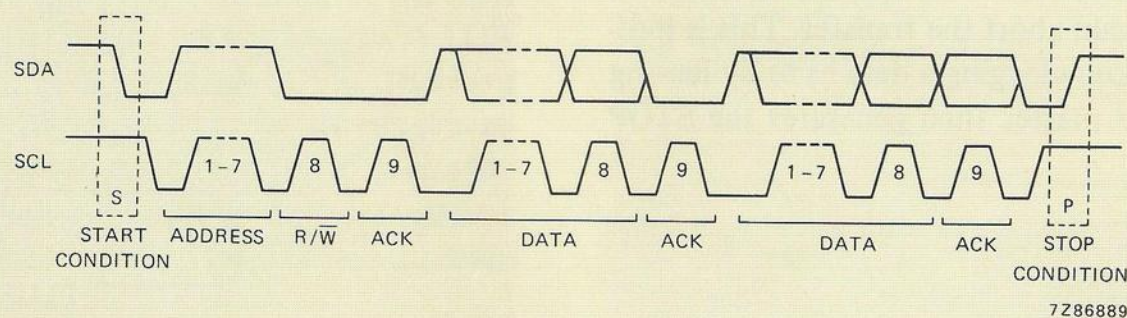
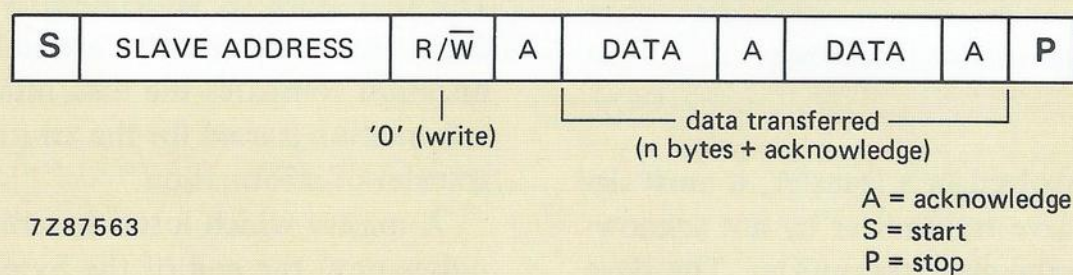


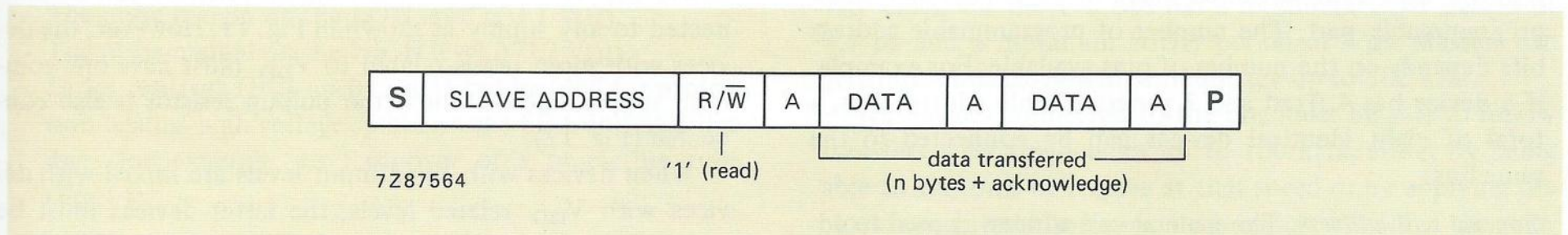
Fig.8 A complete data transfer

another start condition, and address another slave without first generating a stop condition. Various combinations of read/write formats are then possible within such a transfer. Possible data transfer formats are:

(a) Master transmitter transmits to slave receiver. Direction is not changed.

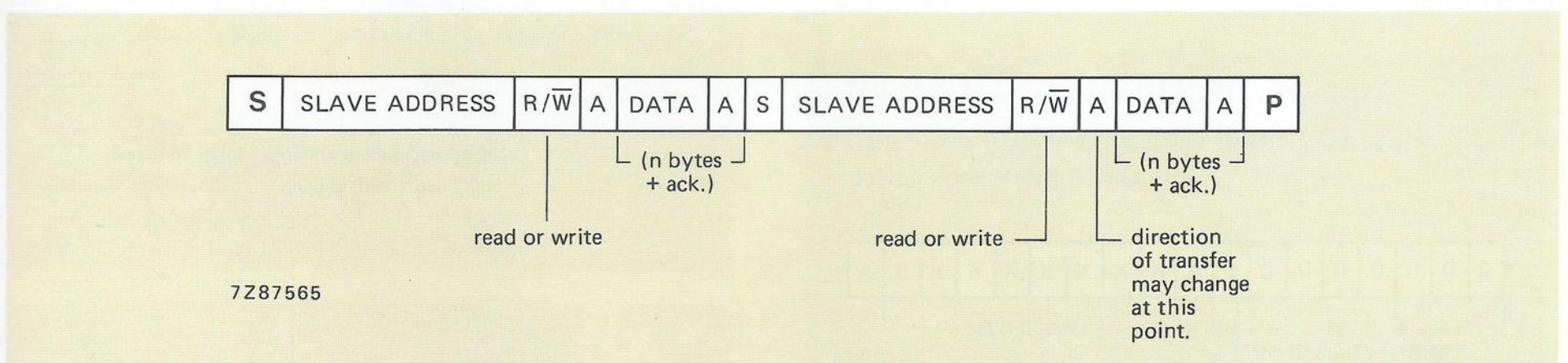


(b) Master reads slave immediately after first byte.



At the moment of the first acknowledge, the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter. This acknowledge is still generated by the slave. The stop condition is generated by the master.

(c) Combined formats.



During a change of direction within a transfer, the start condition and the slave address are both repeated, but with the $R/\bar{W}$ bit reversed.

Notes:

- 1) Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the start condition is repeated, data can be transferred.
- 2) All decisions on auto-increment or decrement of previously accessed memory locations etc. are made by the designer of the device.
- 3) Each byte is followed by an acknowledge as indicated by the A blocks in the sequence.
- 4) I²C devices have to reset their bus logic on receipt of a start condition such that they all anticipate the sending of a slave address.

Addressing

The addressing procedure for the I²C bus is such that the first byte after the start condition determines which slave will be selected by the master. Usually, this first byte follows that start condition. The exception is the 'general call'

address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge, although devices can be made to ignore this address. The second byte of the general call address then defines the action to be taken.

Definition of Bits in the First Byte. The first seven bits of this byte are the slave address (Fig.9). The eighth bit (LSB – least significant bit) determines the direction of the message. A '0' in the least significant position of the first byte means that the master will write information to a selected slave; a '1' in this position means that the master will read information from the slave.

When the address is sent, each device connected to the bus compares the first 7 bits after the start condition with its own address; if there is a match, the device considers itself addressed by the master as a slave receiver or slave transmitter, depending on the $R/\bar{W}$ bit.

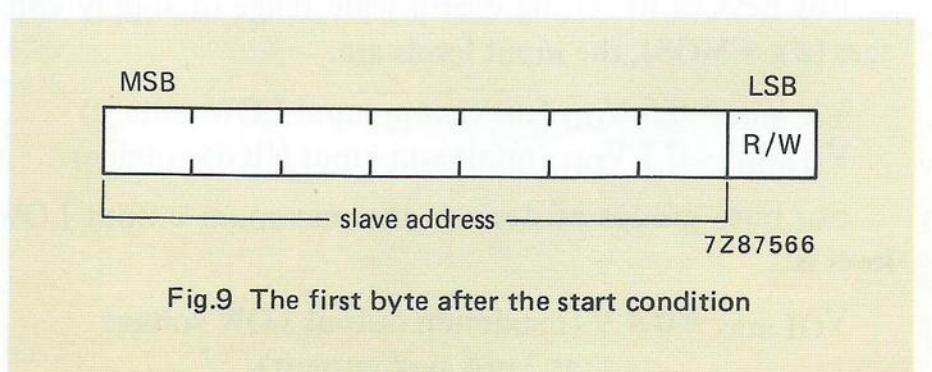


Fig.9 The first byte after the start condition

Since identical ICs may be used more than once in a system the slave address can be made up of a fixed part and a programmable part. The number of programmable address bits depends on the number of pins available. For example, if a device has 4 fixed and 3 programmable address bits, a total of eight identical devices can be connected to the same bus.

General call address. The general call address is used to address every device connected to the I²C bus. However, if a device does not need any of the data supplied within the general call structure, it can ignore this address. If a device does require data from a general call address, it will behave as a slave receiver. The second and following bytes will be acknowledged by every slave receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not acknowledging. The meaning of the general call address is always specified in the second byte (Fig. 10).

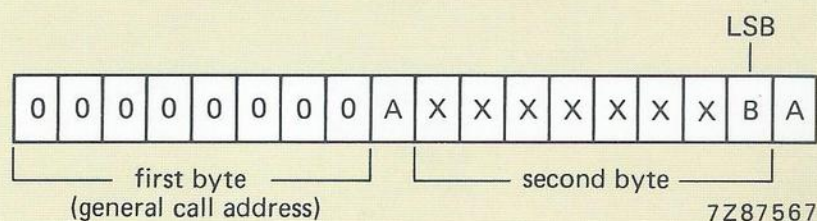


Fig.10 General call address format

ELECTRICAL SPECIFICATIONS OF INPUTS AND OUTPUTS OF I²C DEVICES

The I²C bus allows communication between devices made in different technologies which might also use different supply voltages. For devices operating on a supply voltage of $5\text{ V} \pm 10\%$, the input levels are:

$$V_{IL\max} = 1,5\text{ V (maximum input LOW voltage)}$$

$$V_{IH\min} = 3,0\text{ V (minimum input HIGH voltage)}$$

Devices operating on a supply voltage different from 5 V (e.g. bipolar), must also have these input levels.

For devices operating over a wide range of supply voltages (e.g. CMOS), the input levels are:

$$V_{IL\max} = 0,3 V_{DD} \text{ (maximum input LOW voltage)}$$

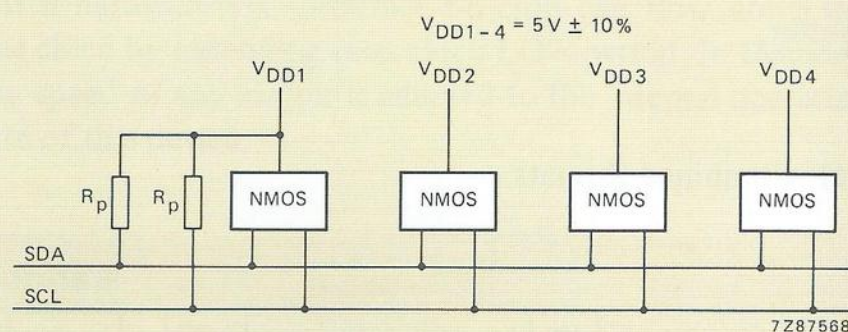
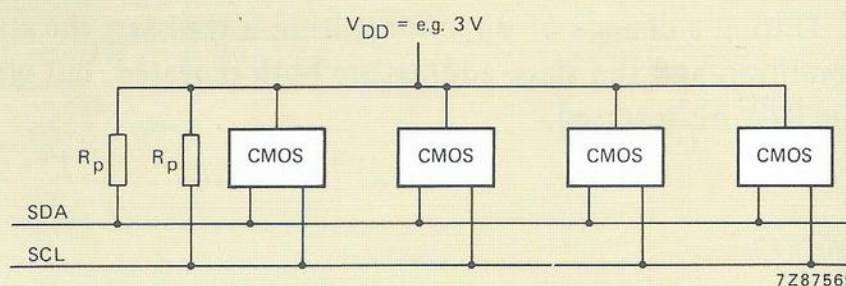
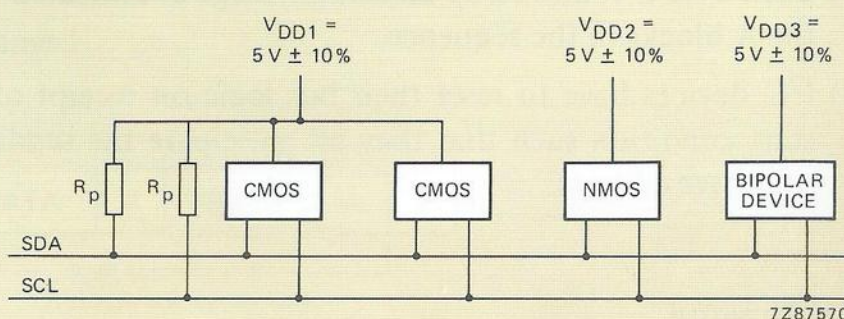
$$V_{IH\min} = 0,7 V_{DD} \text{ (minimum input HIGH voltage)}$$

For both groups of devices, the maximum output LOW level is:

$$V_{OL\max} = 0,4\text{ V (maximum output LOW voltage at 3 mA sink current).}$$

Devices with fixed input levels can each have their own power supply of $5\text{ V} \pm 10\%$. Pull-up resistors can be connected to any supply as shown in Fig. 11. However, the devices with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (Fig. 12).

When devices with fixed input levels are mixed with devices with V_{DD} related levels, the latter devices must be connected to one common supply line of $5\text{ V} \pm 10\%$ along with the pull-up resistors (Fig. 13).

Fig.11 Connection of fixed input level devices to the I²C busFig.12 Connection of devices with a wide supply voltage range to the I²C busFig.13 Connection of a mixture of devices with fixed input levels and devices with supply voltage related input levels to the I²C bus

Input levels are defined in such a way that:

- The noise margin on the LOW level is $0,1 V_{DD}$.
- The noise margin on the HIGH level is $0,2 V_{DD}$.
- Series resistors (R_S) up to 300Ω can be used for protection against high voltage spikes on the SDA and SCL line due, for example, to flash-over of a tv picture tube (Fig.14).

The maximum bus capacitance per wire is 400 pF . This includes the capacitance of the wire itself and the capacitance at the pins connected to it.

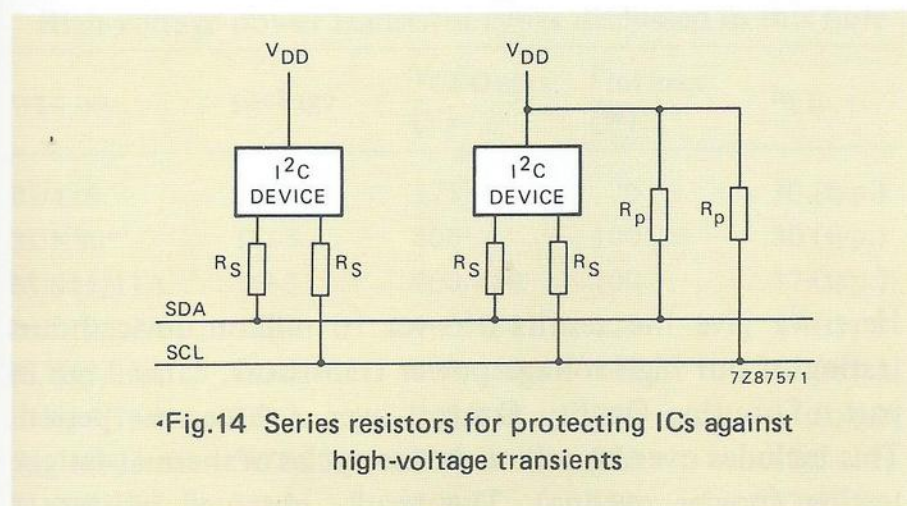


Fig.14 Series resistors for protecting ICs against high-voltage transients

TIMING

The clock on the I²C bus has a minimum LOW period of $4,7 \mu\text{s}$ and a minimum HIGH period of $4 \mu\text{s}$. Masters can generate a bus clock with a frequency up to 100 kHz .

All devices connected to the bus must be able to follow transfers with frequencies up to 100 kHz , either by being able to transmit or receive at that speed or by applying the clock synchronisation procedure which will force the master into a wait state and stretch the LOW periods. Of course, in the latter case the frequency is reduced.

FURTHER INFORMATION

Further information is available in the I²C bus specification, ordering code 9398 615 00011.

Authors

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Ir. A.P.M. Moelands



August Petersen, was born near Flensburg, Germany, in 1937, and graduated in physics from the University of Kiel in 1964. The same year he joined Valvo Application Laboratory, Hamburg, initially working on applications of passive components, especially piezo-electric ceramics. As a member of the Industrial Electronics Group, he is currently responsible for developing sensor control circuitry.



Andreas D. Schelling was born in Dussnang, Switzerland in 1953. He received an MSc in electrical engineering from the Federal Institute of Technology, Zurich, after which he worked for a time at Nippon Telephone and Telegraph, Japan. In 1982 he joined Videlec — a joint Philips/Brown Boveri venture in Lentzburg, Switzerland, and is currently responsible for technical sales support of liquid crystal displays.



J. Dijk was born in Zuidlaren, The Netherlands in 1946. He studied electronics at Groningen, completing his studies in 1967. In 1970 he joined Philips' Quality Laboratory for Semiconductors, Stadskanaal, and is currently working in the area of power transistors.



Helfried Schmickl studied mechanical and electrical engineering and took his doctorate at the University of Technology, Graz, Austria, in 1970. After working on capacitor development for Siemens G.m.b.H., Deutschlandberg, he joined Philips in 1973 and since 1977 has been in charge of electrolytic capacitor development, first at Klagenfurt and, since 1979, as development chief at Zwolle. He is a reader in television engineering at the University of Technology, Graz.



Wil J.W. Kitzen was born in Grevenbicht, The Netherlands in 1955. He studied electrical engineering at Eindhoven University of Technology, receiving his MSc in 1979. The same year he joined Philips Research Laboratories, Eindhoven, initially working on loudspeaker arrays, dummy-head stereophony and room acoustics. Since 1980 he has worked on digital signal processing techniques in the field of electro-acoustics.



Just W.H. Slakhorst received his degree in materials science from Twente University of Technology in 1973, and his doctorate from the Dutch Foundation for Fundamental Research of Matter, in 1977. The same year he also received the Brandoma Award for his work on recrystallization textures. He joined Philips Elcoma Division, Zwolle in 1978, and is currently responsible for development of wet electrolytic capacitors and for production of capacitor foils.

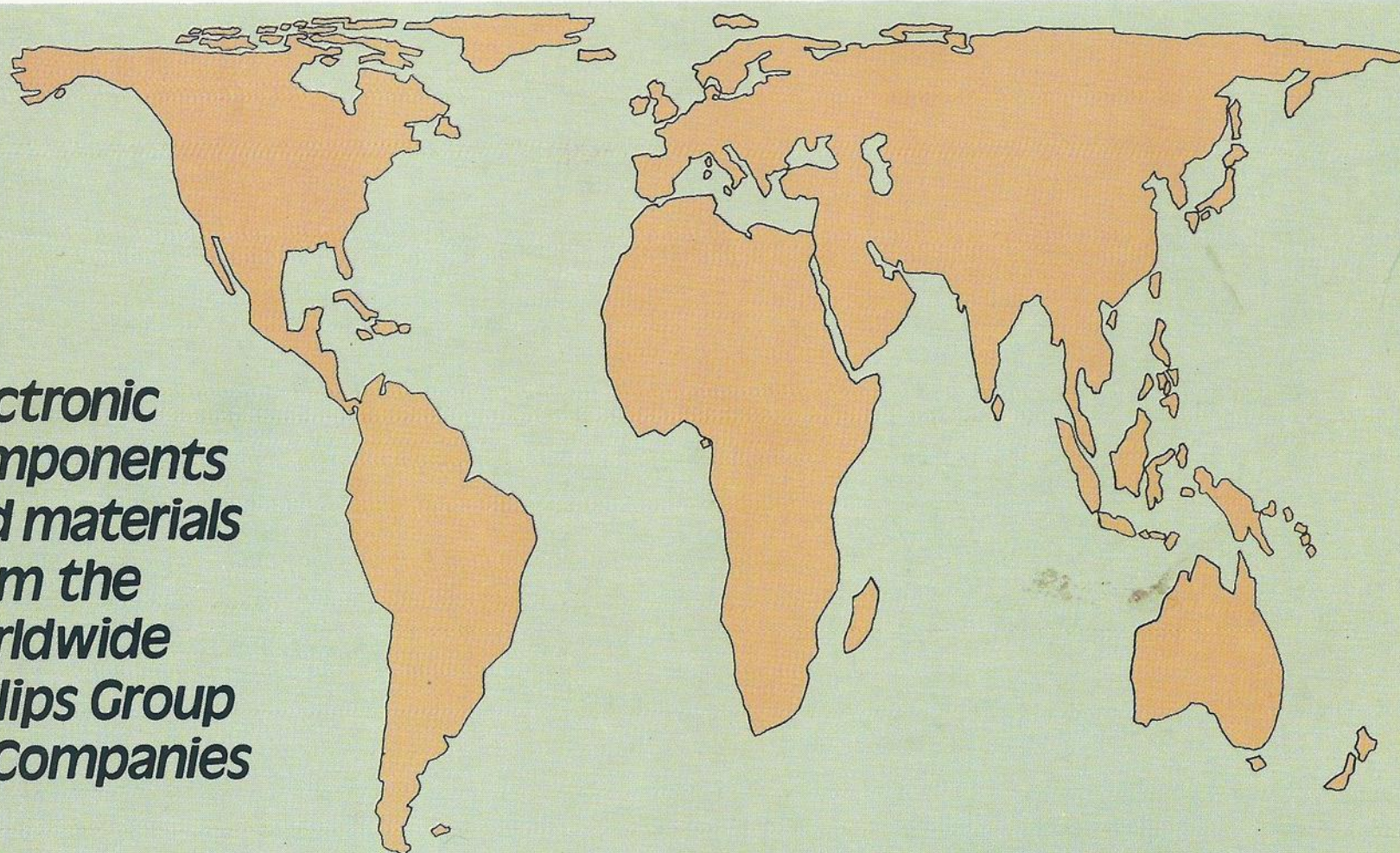


A.P.M. Moelands was born at Breda, The Netherlands, in 1951. After graduating in electrical engineering at the University of Technology, Eindhoven, in 1976, he joined Philips Electronic Components and Materials Division where he was instrumental in the development of the 8400 serial I/O. He is now a member of the product marketing group *MOS microprocessors*.



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