



Electronic
components
and materials

PHILIPS



THE INTER IC BUS



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MOS Microprocessors

THE I²C BUS IS A SERIAL DATA BUS FOR USE BETWEEN
ICs AND / OR MODULES.

THE I²C BUS CONSISTS OF TWO WIRES:

A DATA WIRE SDA AND A CLOCK WIRE SCL.



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DESIGN STARTING POINTS I²C

1. SERIAL DATA TRANSFER

- REDUCTION OF INTERCONNECTION COSTS
- SIMPLER PRINTED CIRCUIT BOARD DESIGN
- SMALLER CONNECTORS ON MODULES
- LESS PINS ON INTEGRATED CIRCUITS



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DESIGN STARTING POINTS I²C

2. BIDIRECTIONAL DATA TRANSFER WITH ACKNOWLEDGE

- FUNCTIONAL REQUIREMENT FOR E.G. RAM
- ACKNOWLEDGEMENT FOR CHECK ON DATA TRANSFER
- DETERMINATION OF SYSTEM CONFIGURATION



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DESIGN STARTING POINTS I²C

3. MULTIMASTER CAPABILITY

- MODULAR SYSTEM BUILD-UP HW/SW
- LOCAL PROCESSING OF REAL TIME TASKS
- NO CENTRAL MASTER
- REDUCTION IN BUS OCCUPATION
- EXPANDABILITY
- POSSIBILITY OF DIAGNOSTIC / ADJUSTMENT PROCEDURES



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DESIGN STARTING POINTS I²C

4. ADDRESSING OF SLAVE IN PROTOCOL

- ELIMINATION OF ENABLE LINES
- MORE I/O PINS LEFT ON CONTROLLER



DESIGN STARTING POINTS I²C

5. SIMPLE IMPLEMENTATION

- SLAVE IMPLEMENTATION REQUIRES NO CLOCK
- COMPETITIVE WITH LOW COST SYSTEMS
- CLOCK GENERATION BY MASTER



THE I²C BUS

APPLICATION AREAS

- VIDEO
- AUDIO
- DOMESTIC APPLIANCES
- TELEPHONY
- AUTOMOTIVE
- INSTRUMENTATION
- INDUSTRIAL CONTROL



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CHARACTERISTICS I²C BUS

1. TWO-WIRE SERIAL BIDIRECTIONAL BUS
2. ACKNOWLEDGEMENT AFTER EACH TRANSFERRED BYTE
3. REAL MULTIMASTER CAPABILITY
4. DATA RATE OF UP TO 100 KBITS/SEC
5. MAX. DRIVE CAPACITY OF 400 pF
6. SLAVE SELECTION IN PROTOCOL
7. DURATION OF TRANSFER NOT FIXED



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THE I²C BUS

DEFINITIONS

THE MASTER IS THE DEVICE THAT:

- A. TAKES THE INITIATIVE TO START A TRANSFER
- B. GENERATES THE CLOCK
- C. SELECTS THE SLAVE
- D. CAN BE TRANSMITTER OR RECEIVER
- E. TERMINATES THE TRANSFER

THE SLAVE IS THE DEVICE THAT:

- A. IS SELECTED BY THE MASTER
- B. IS CONTROLLED BY THE MASTER CLOCK
- C. CAN BE RECEIVER OR TRANSMITTER



THE I²C BUS

- EACH TRANSFER CONSISTS OF N BYTES
(N NOT RESTRICTED)
- EACH BYTE IS FOLLOWED BY A NINTH
ACKNOWLEDGEMENT BIT
- THE FIRST BYTE CONTAINS THE SLAVE ADDRESS AND
THE DIRECTION BIT
- A CHANGE OF DIRECTION WITHIN A TRANSFER IS
POSSIBLE BY REPEATING THE START CONDITION



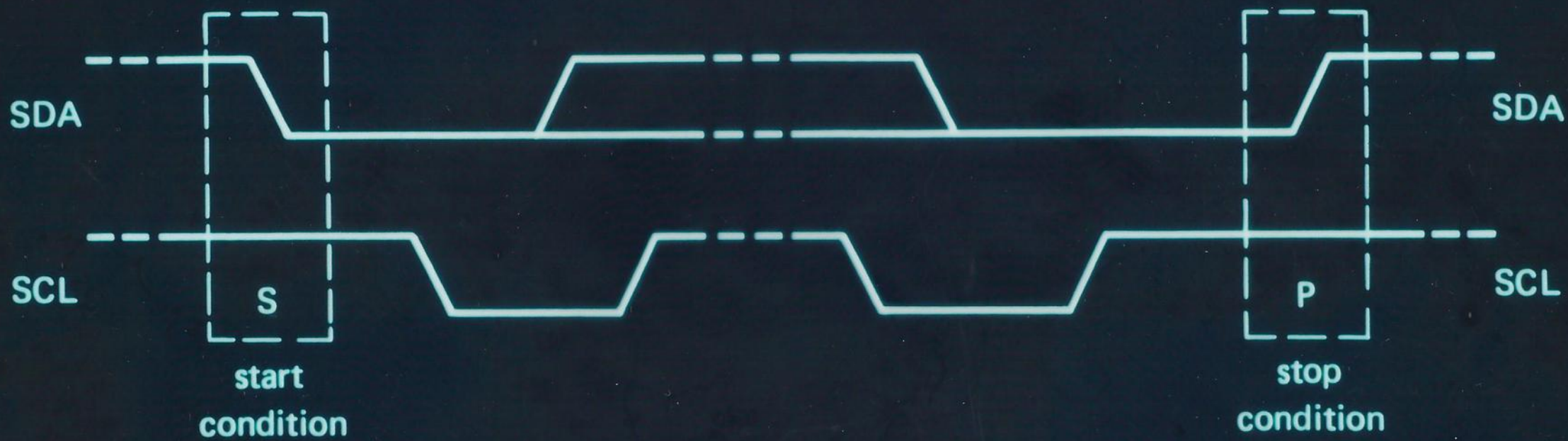
THE I²C BUS

- WHEN THE I²C BUS IS NOT IN USE BOTH THE DATA LINE SDA AND THE CLOCK LINE SCL HAVE THE HIGH LEVEL
- DURING A TRANSFER THE DATA LINE IS ONLY ALLOWED TO CHANGE IF THE CLOCK LINE HAS THE LOW LEVEL
- TRANSITIONS OF THE DATA LINE WHILE THE CLOCK LINE IS HIGH ARE DEFINED AS START AND STOP CONDITIONS



THE I²C BUS

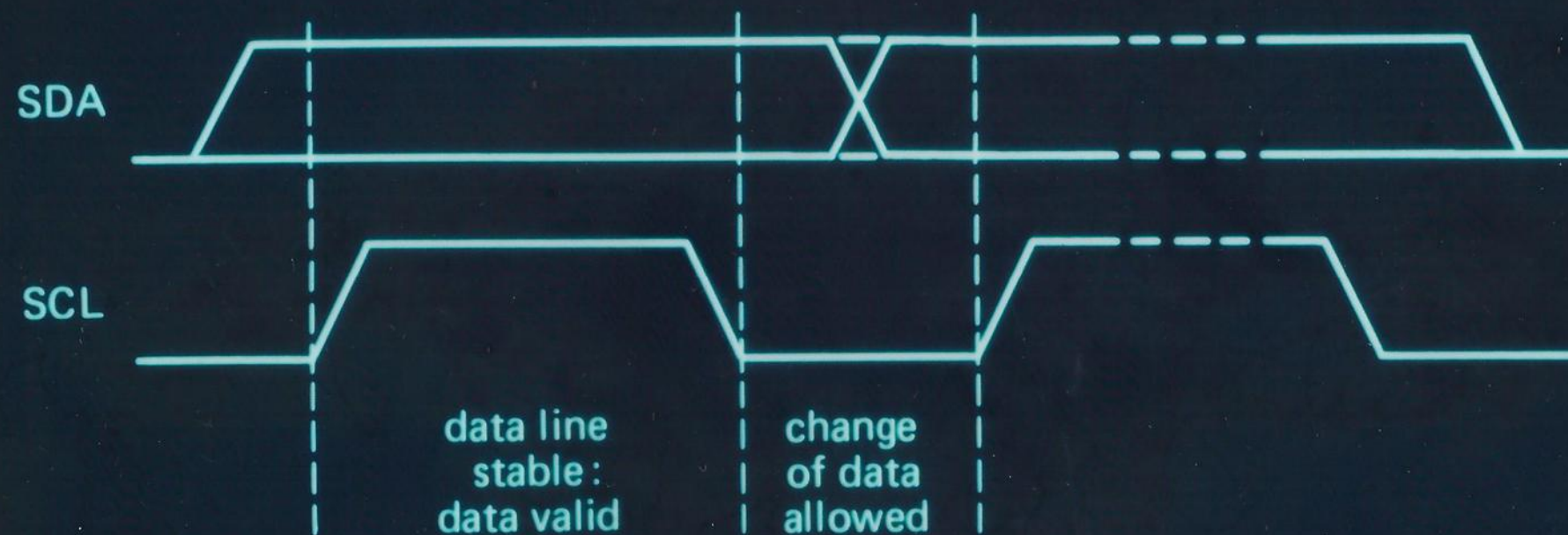
START AND STOP CONDITIONS



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BIT TRANSFER ON THE I²C BUS



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THE I²C PROTOCOL DOES NOT CONTAIN AN END OF DATA BIT

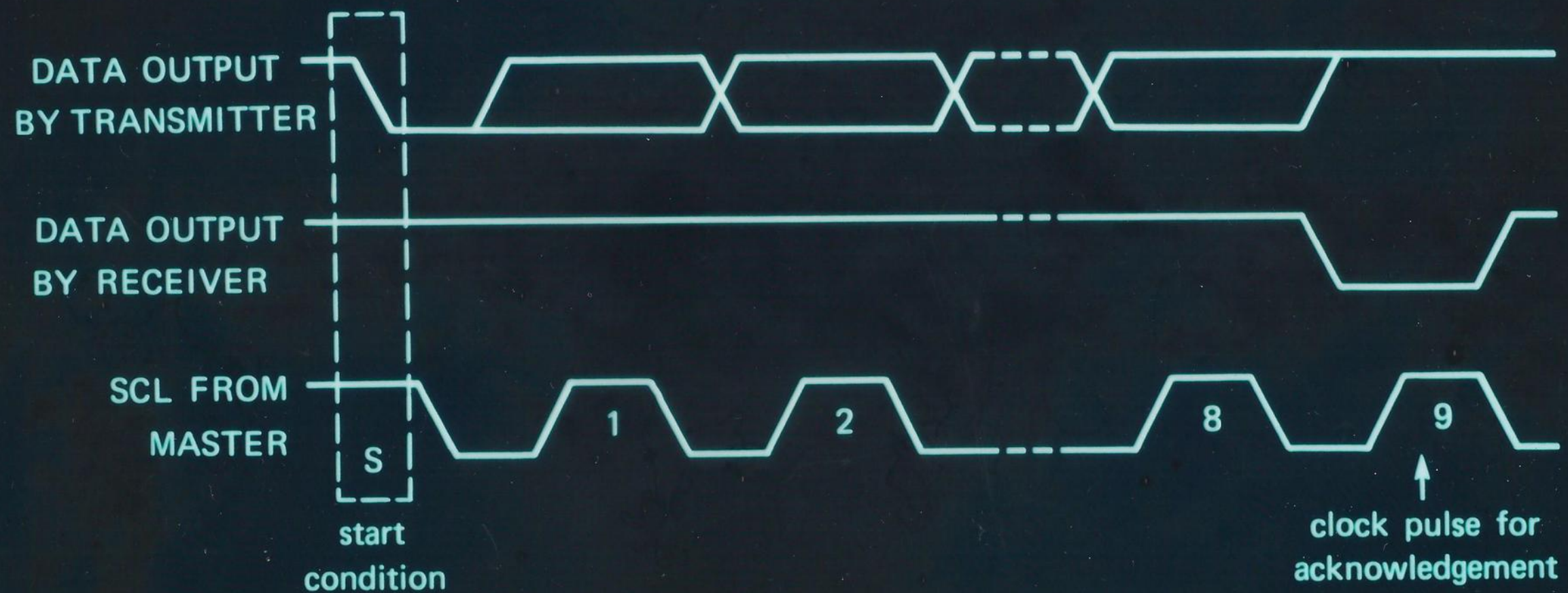
WHEN A MASTER RECEIVER WANTS TO TERMINATE A MESSAGE A NEGATIVE ACKNOWLEDGE IS GIVEN AFTER THE LAST RECEIVED BYTE

A SLAVE TRANSMITTER THAT DOES NOT RECEIVE AN ACKNOWLEDGE ON A BYTE JUST TRANSMITTED HAS TO LEAVE THE DATA LINE HIGH



THE I²C BUS

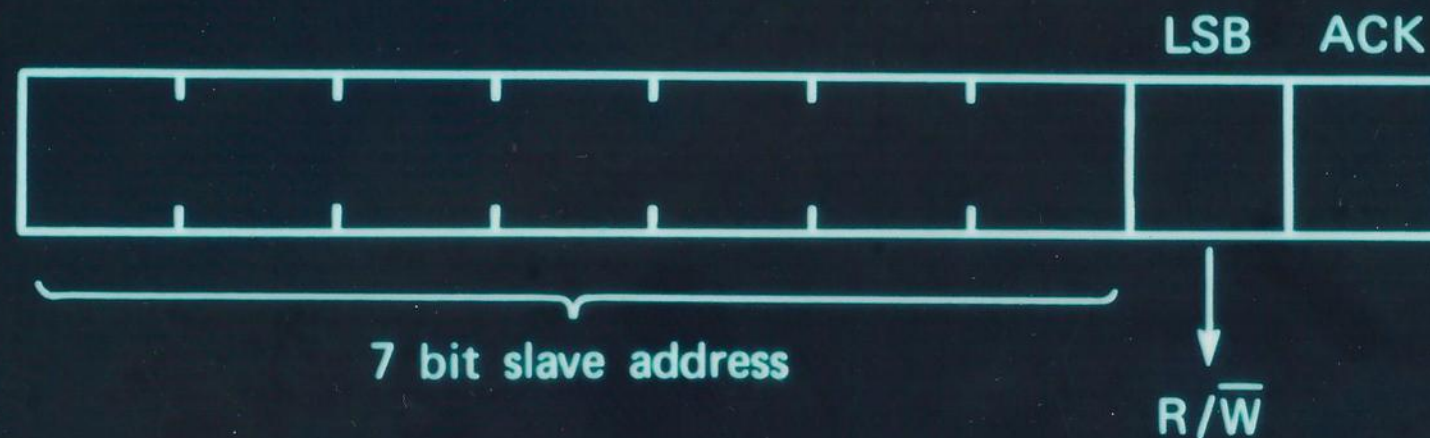
ACKNOWLEDGEMENT ON THE I²C BUS



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FIRST BYTE IN DATA TRANSFER ON THE I²C BUS



0: slave will be written by master

1: slave will be read by master



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FORMAT ON THE I²C BUS

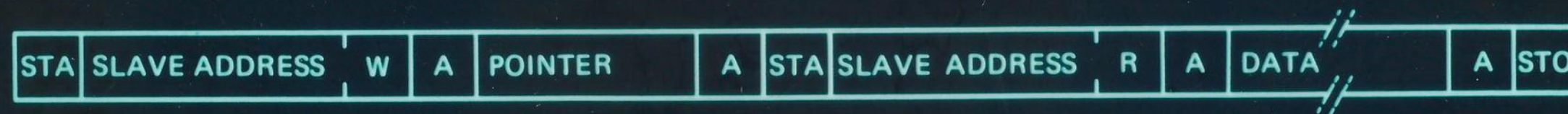


- MASTER TRANSMITTER TRANSMITS DATA TO SLAVE RECEIVER



↑
change of direction

- MASTER READS SLAVE IMMEDIATELY AFTER FIRST BYTE



- MASTER READS SLAVE AFTER SETTING POINTER IN SLAVE



THE I²C BUS

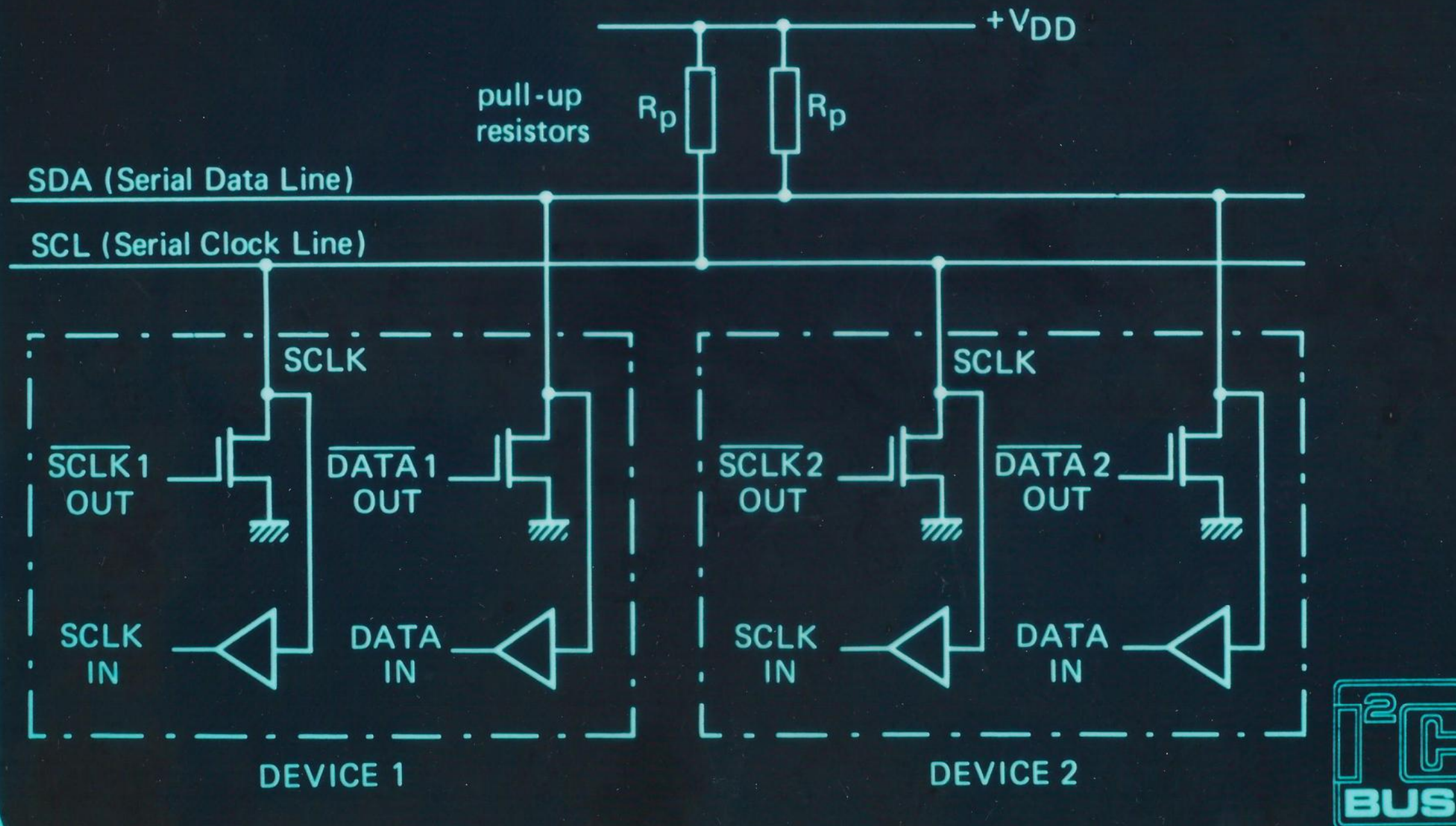
- DEVICES CONNECTED TO THE BUS MUST HAVE AN OPEN DRAIN OR OPEN COLLECTOR OUTPUT
- THE DEVICES MUST BE ABLE TO READ THE STATUS OF THIS OUTPUT



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THE I²C BUS

OUTPUT/INPUT CONFIGURATION



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THE I²C BUS

MULTIMASTER CAPABILITY

- IN CASE OF SIMULTANEOUSLY STARTING MASTERS AN ARBITRATION PROCEDURE IS INVOKED IN WHICH:
 1. THE DIFFERENT CLOCKS ARE SYNCHRONISED
 2. THE DATA IS PROTECTED AGAINST CORRUPTION
- THE ARBITRATION PROCEDURE DOES NOT HANDLE THE PRIORITY IN THE SYSTEM



THE I²C BUS

THE CLOCK SYNCHRONISATION IS USED FOR :

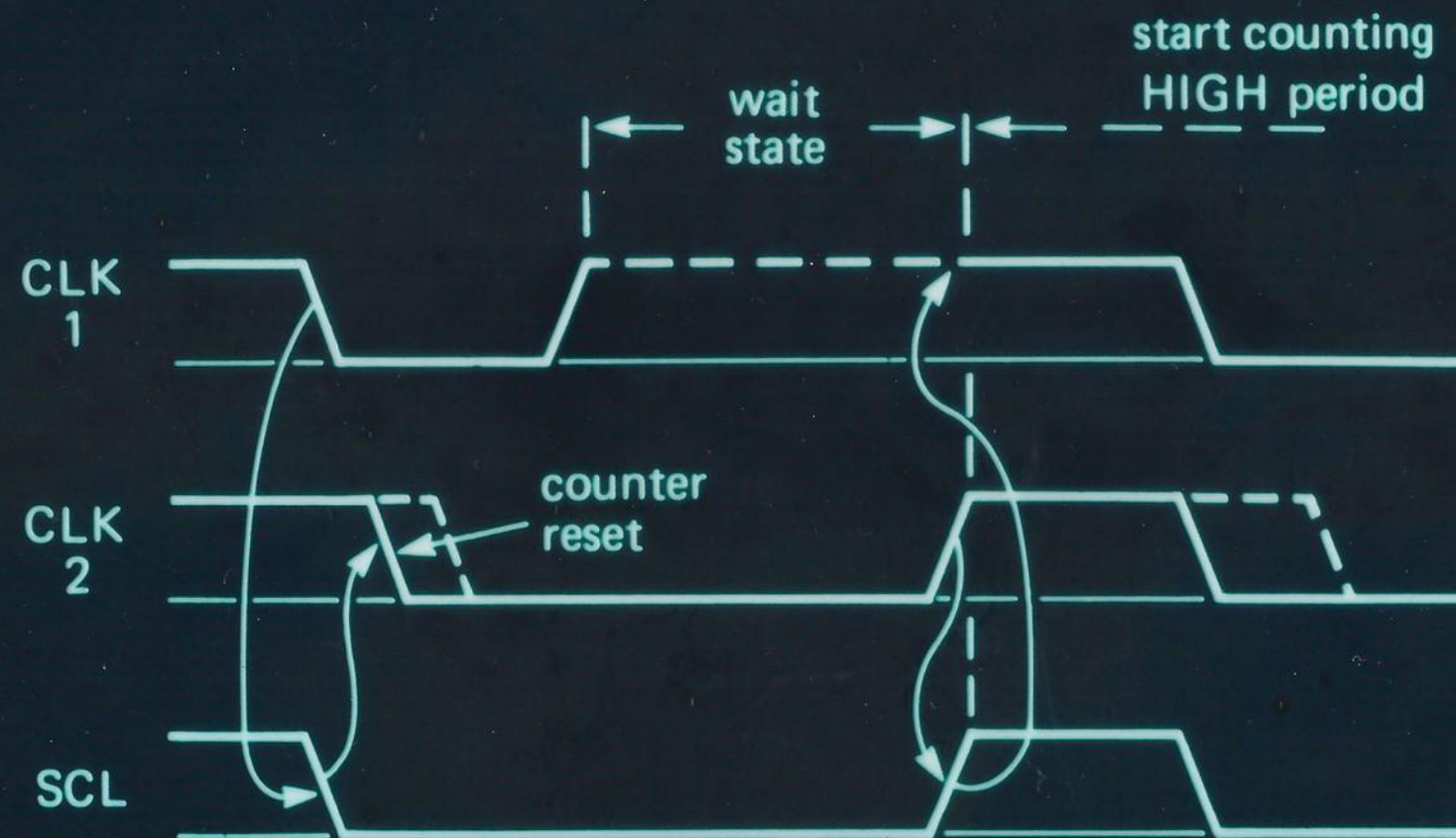
1. SYNCHRONISATION OF CLOCKS OF ARBITRATING MASTERS
2. SYNCHRONISATION OF BUS PARTICIPANTS WITH DIFFERENT PROCESSING SPEEDS



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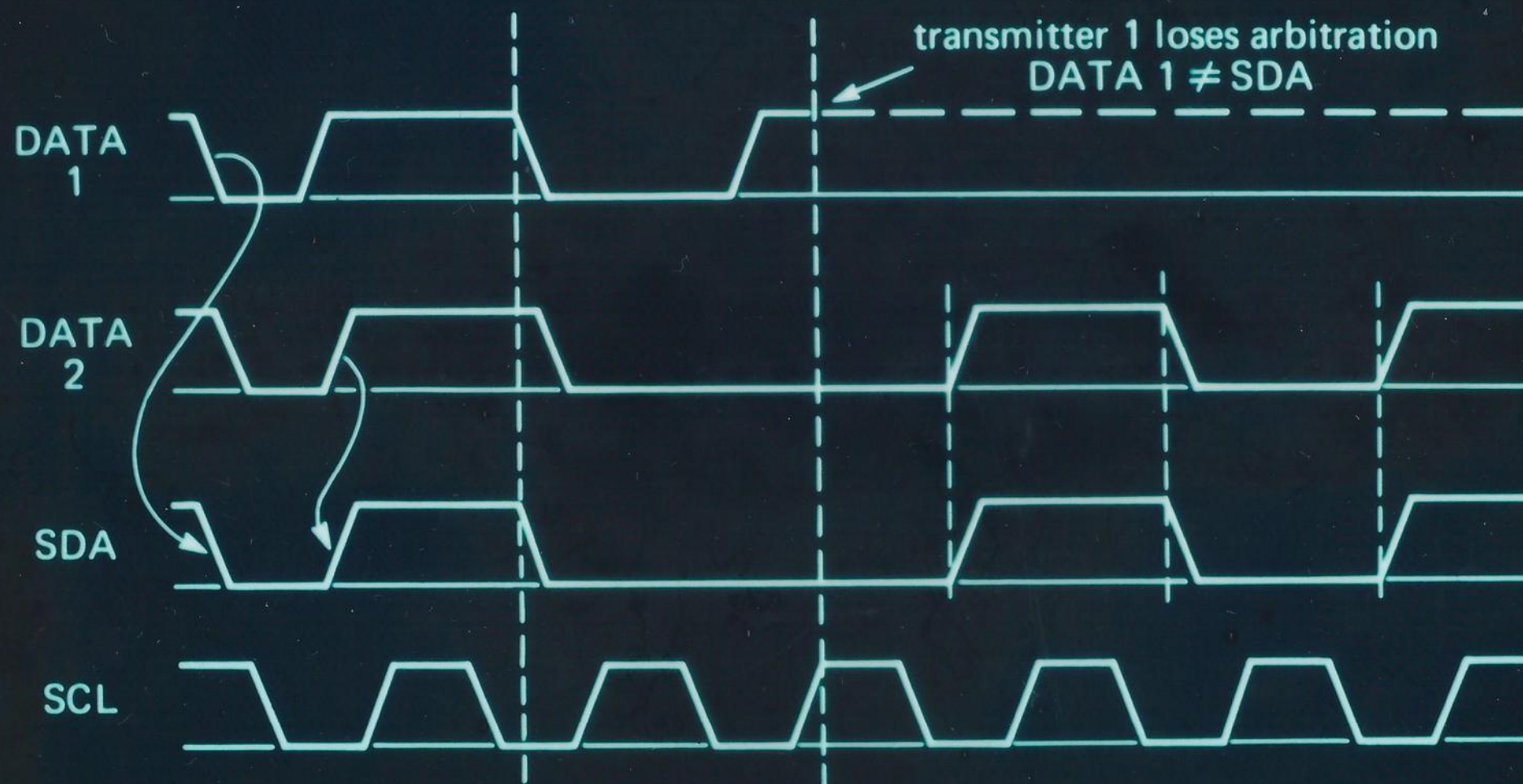
THE I²C BUS

CLOCK SYNCHRONISATION DURING THE ARBITRATION PROCEDURE



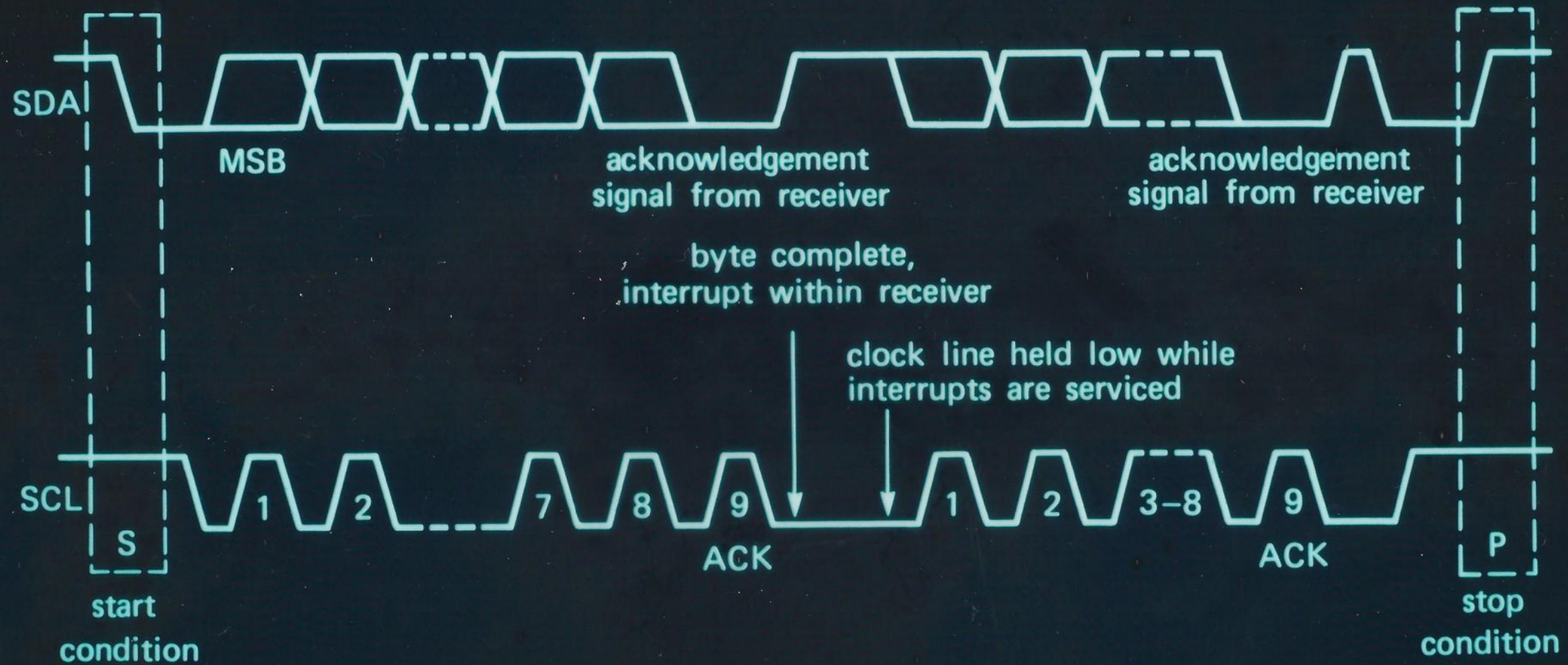
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ARBITRATION PROCEDURE OF TWO MASTERS



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DATA TRANSFER ON THE I²C BUS

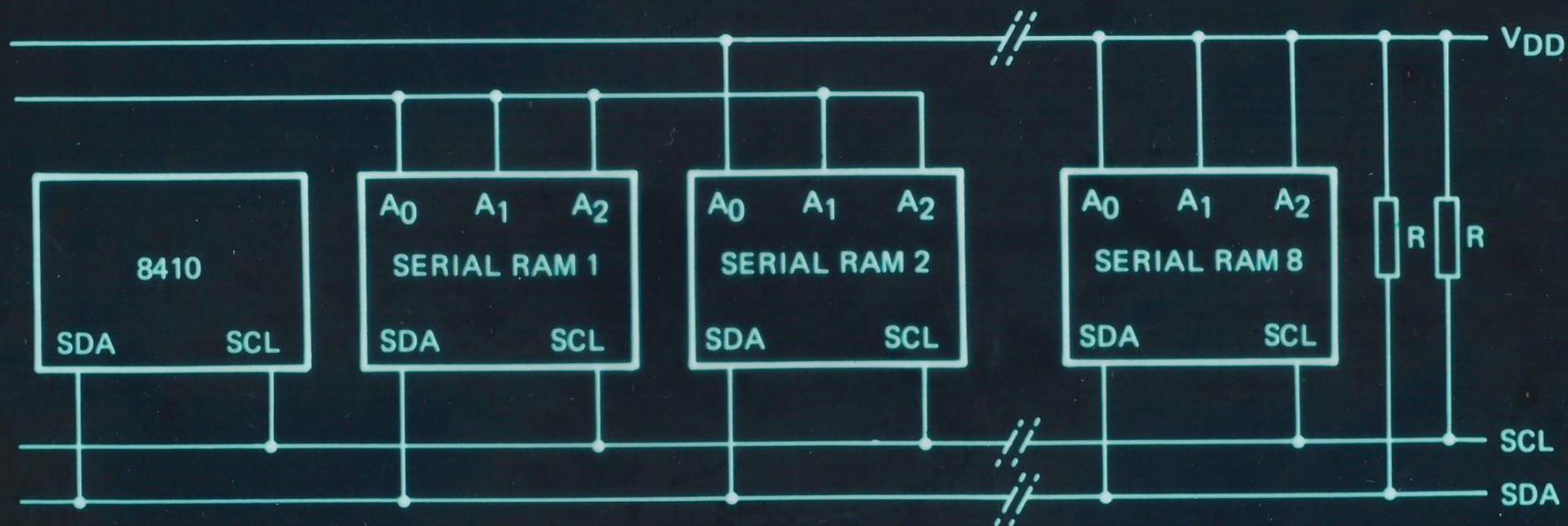


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THE I²C BUS

PROGRAMMING POSSIBILITIES OF I²C HARDWARE PERIPHERALS

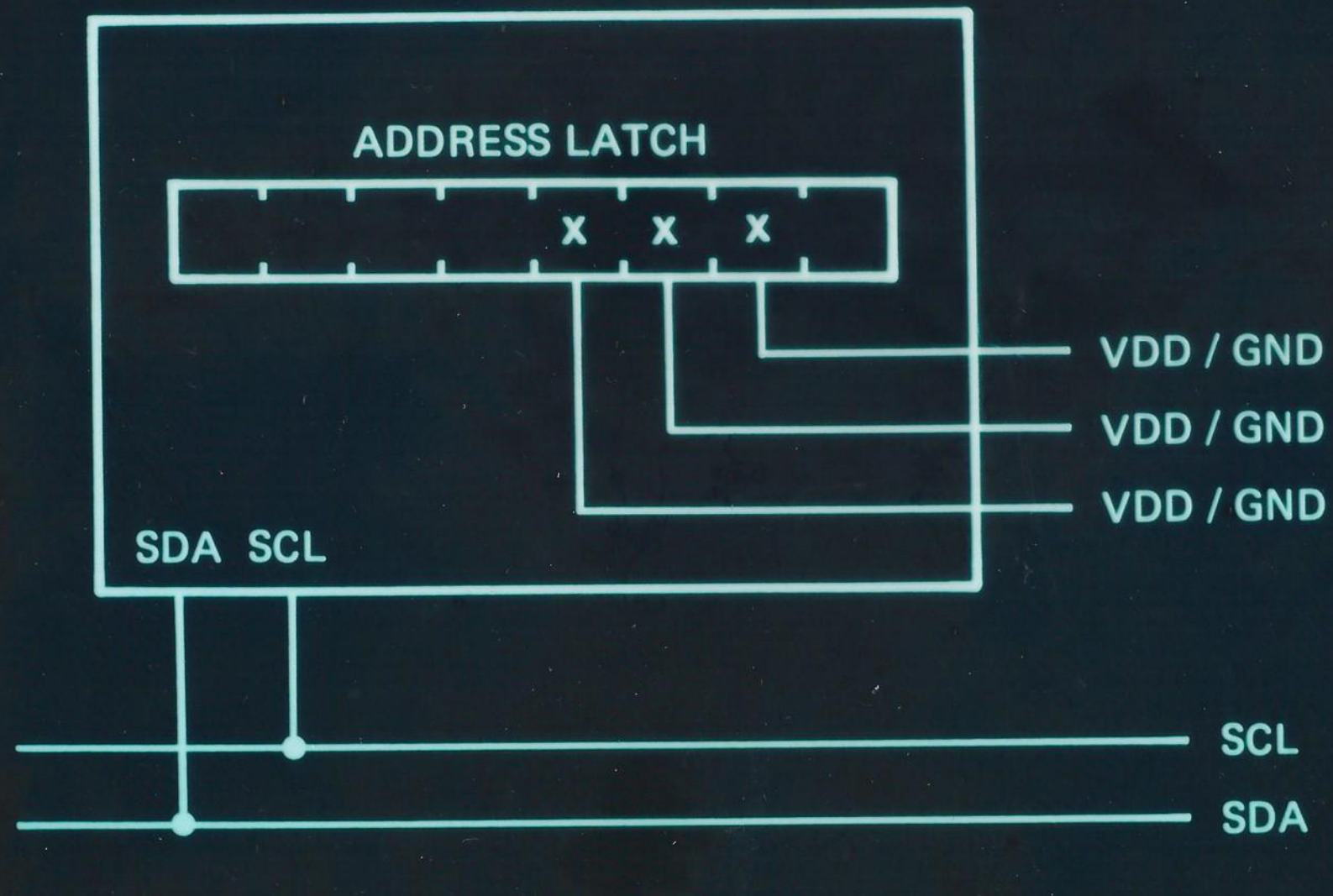
- UNUSED PINS



THE I²C BUS

PROGRAMMING POSSIBILITIES OF I²C HARDWARE PERIPHERALS

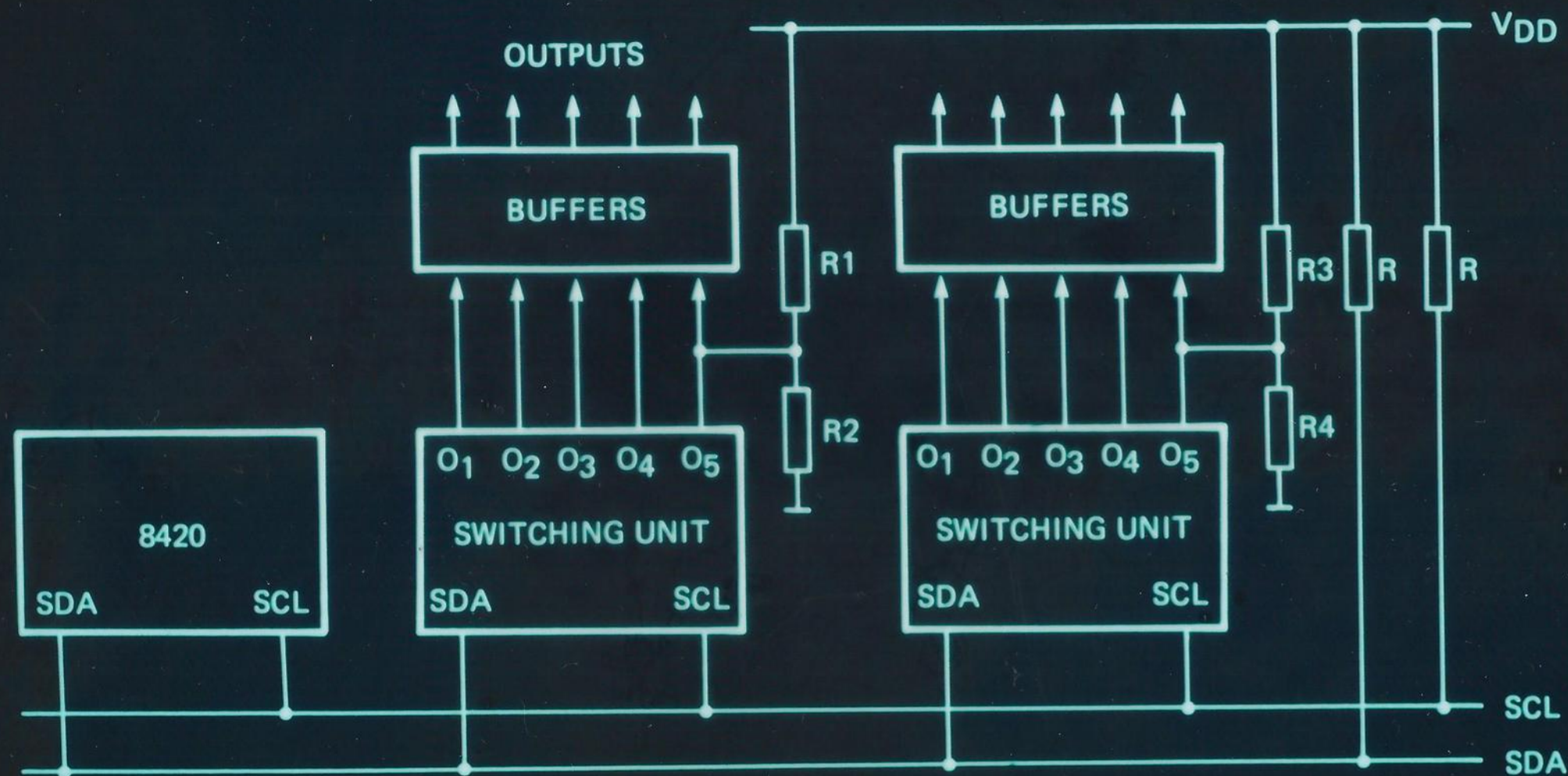
- UNUSED PINS



THE I²C BUS

PROGRAMMING POSSIBILITIES OF I²C HARDWARE PERIPHERALS

- A/D – CONVERSION ON OUTPUT PIN



THE I²C BUS

PROGRAMMING POSSIBILITIES OF I²C HARDWARE PERIPHERALS

- A/D – CONVERSION ON OUTPUT PIN

